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ITX:170*170

Ver: 12

Intel -SkyLake-S 65W plamform

CPU:

LGA1151
CPU POWER PAK *3 Phase
GT POWER PAK *2 Phase

System Chipset:

SPT-H :B150 colay H110 colay H170

Onboard Chip:

HD Audio Codec: ALC887
SIO: NCT5563D
Flash ROM: SPI 128 MB or 64MB

PWM:

VCORE - RT3606
DDR - RT8231
PCH(1.0V) - RT8125E
VCCSA - RT8125E

Main Memory:

DDR4 * 2 (Dual Channel)

Load Switch:


VCCIO - SLG59M1457V 6A

ACPI:

5VDAUL:uP7501
5VDIMM:uP7501
3VSB:GS7133+PN MOS
3VDSW:GS7133
VCCSTPLL - GS7133

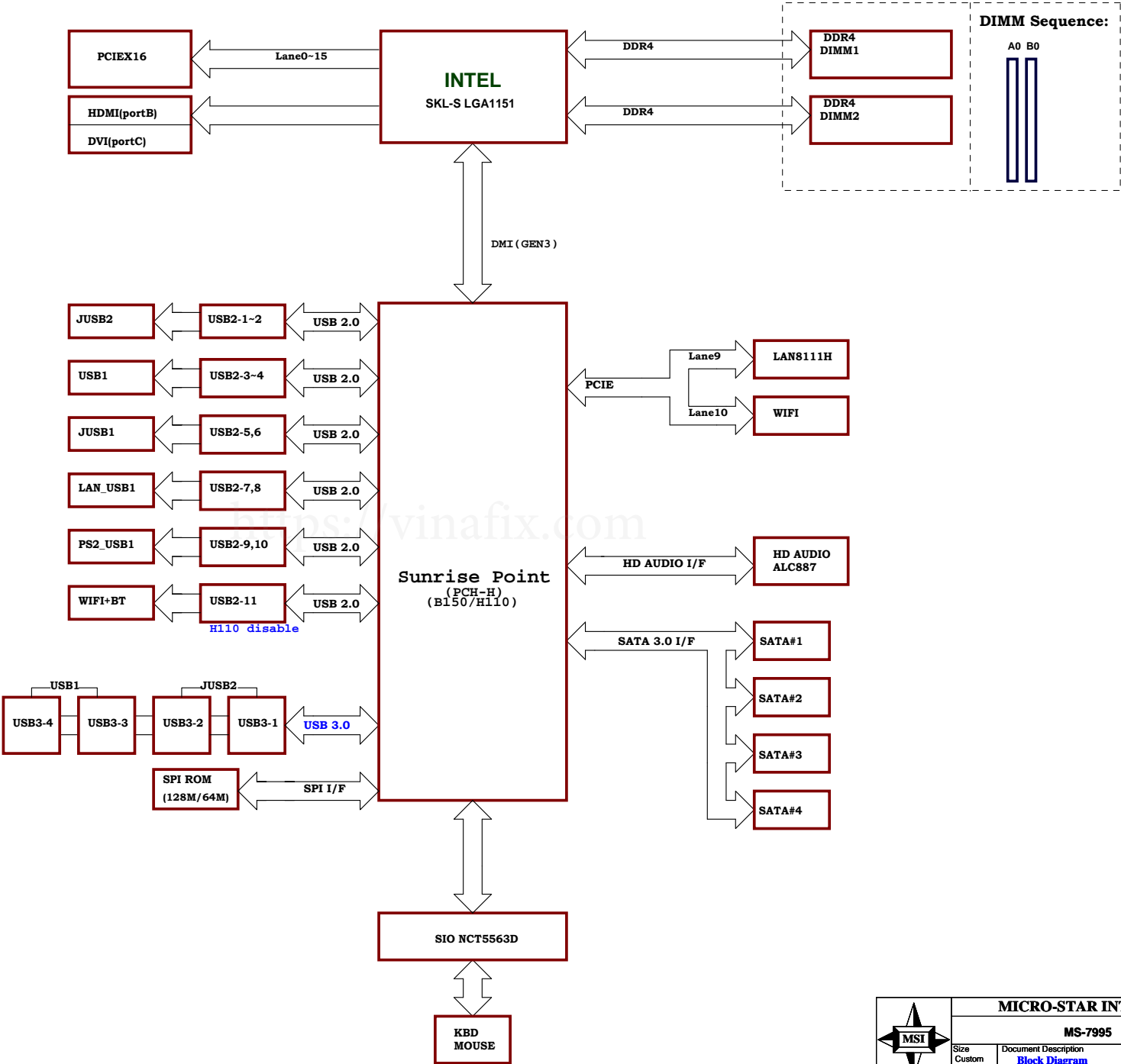
Expansion Slots:

PCI Express (X16) Slot * 1

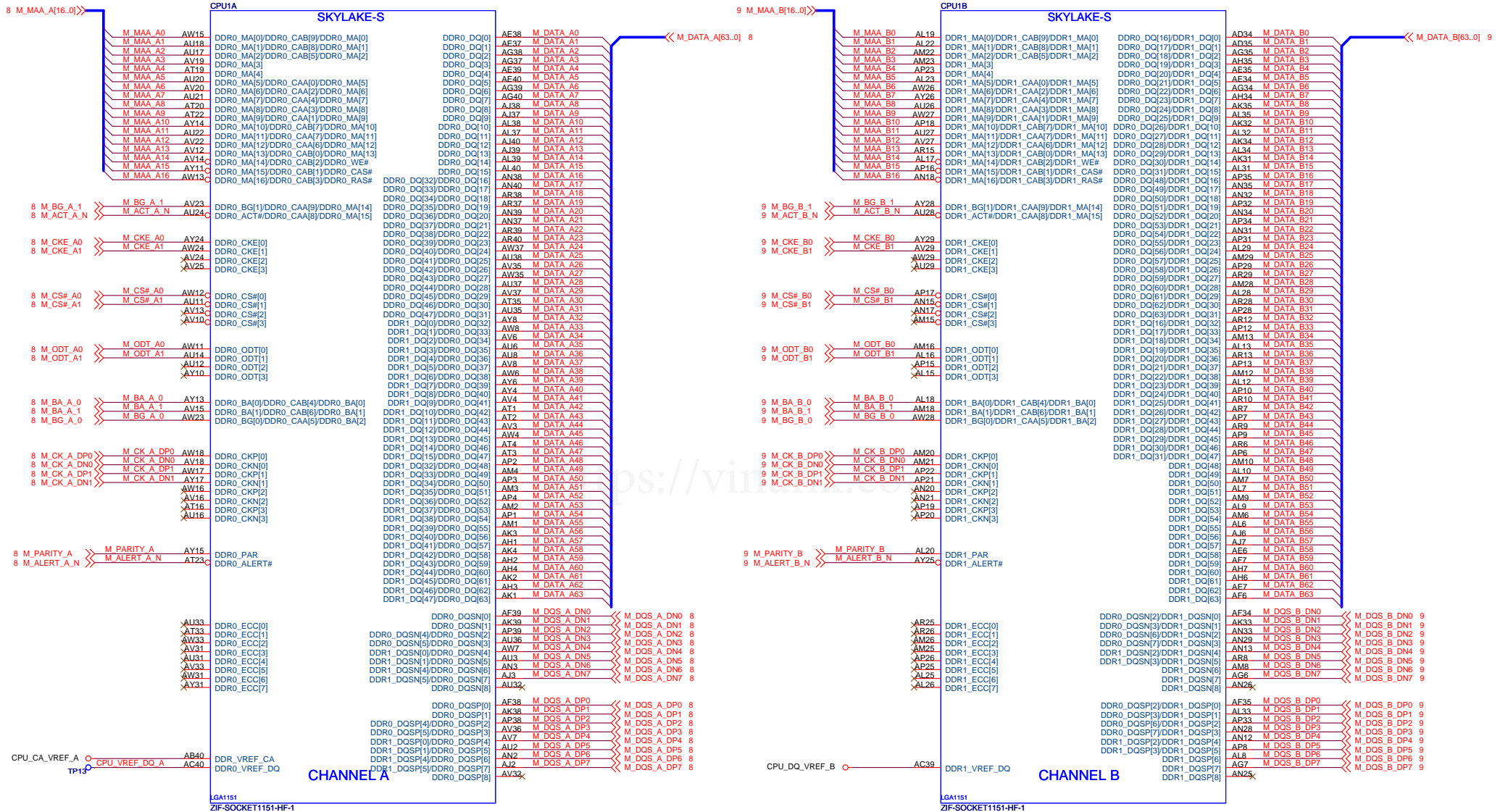


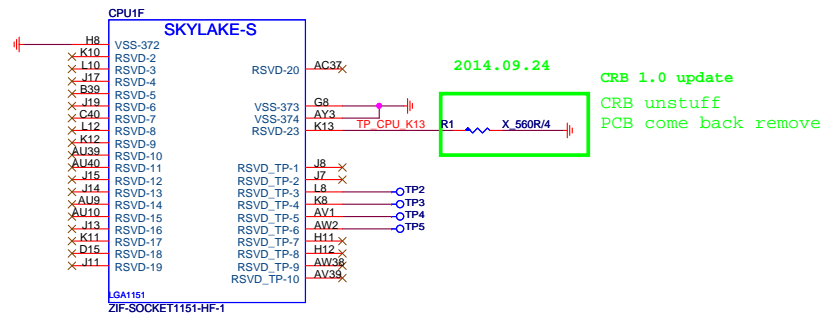
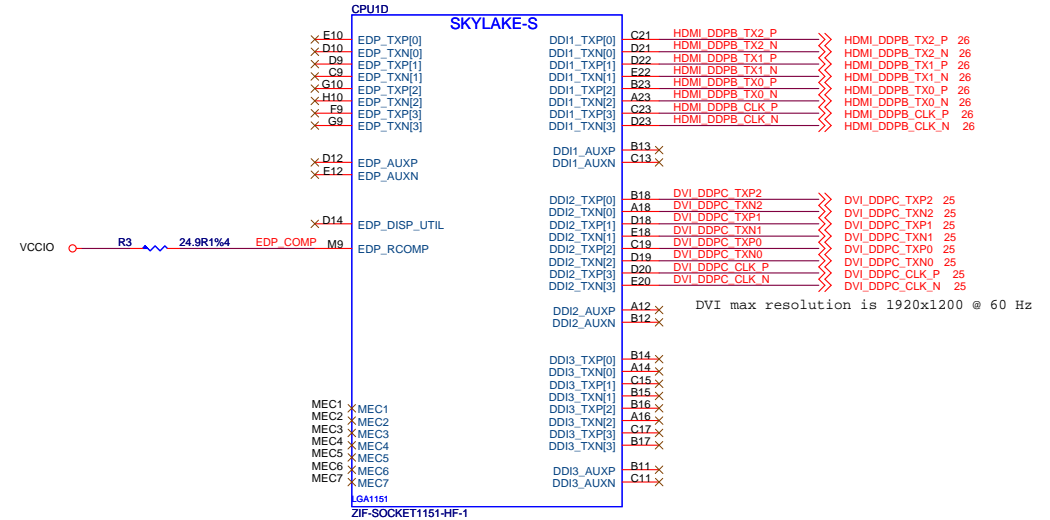
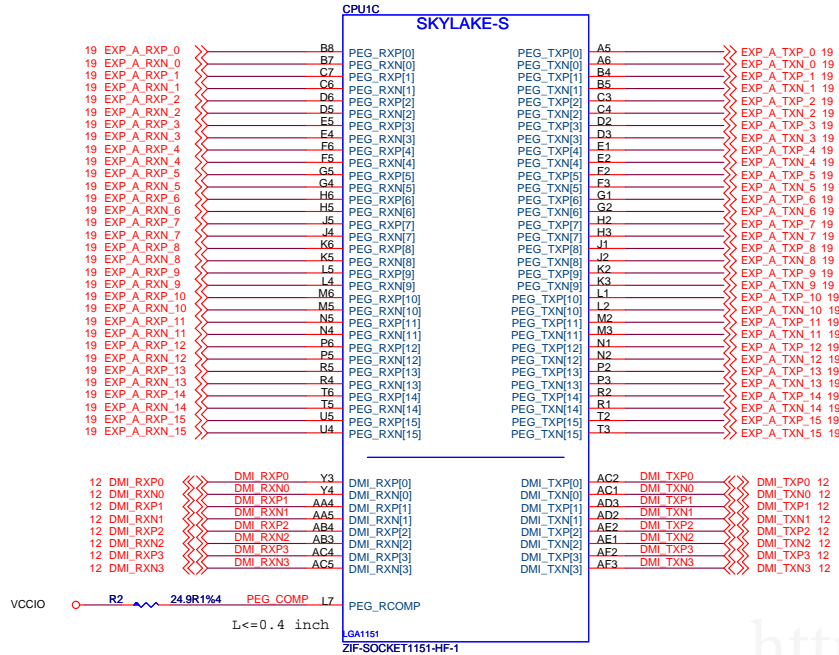
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MS-7995 Block Diagram

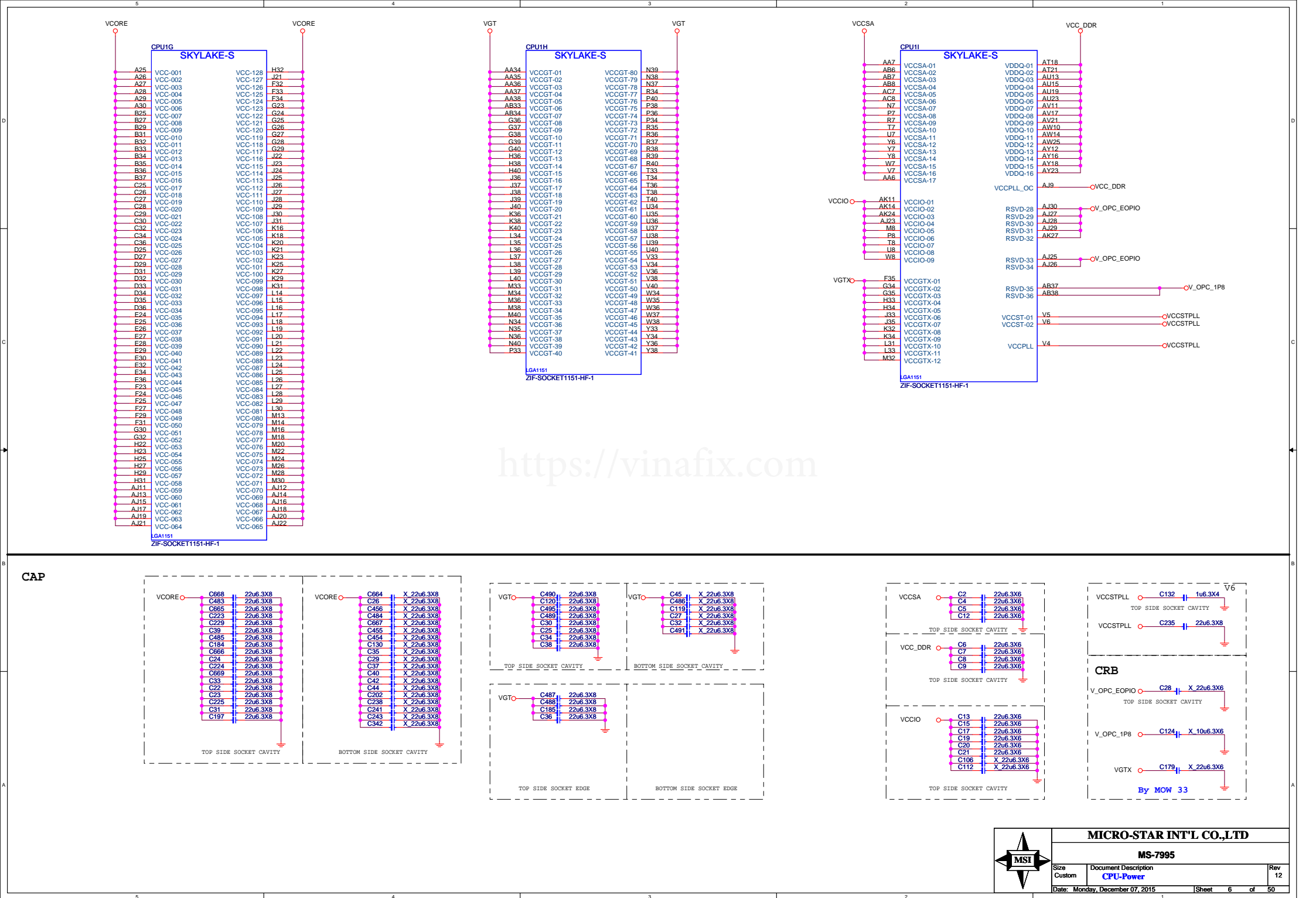


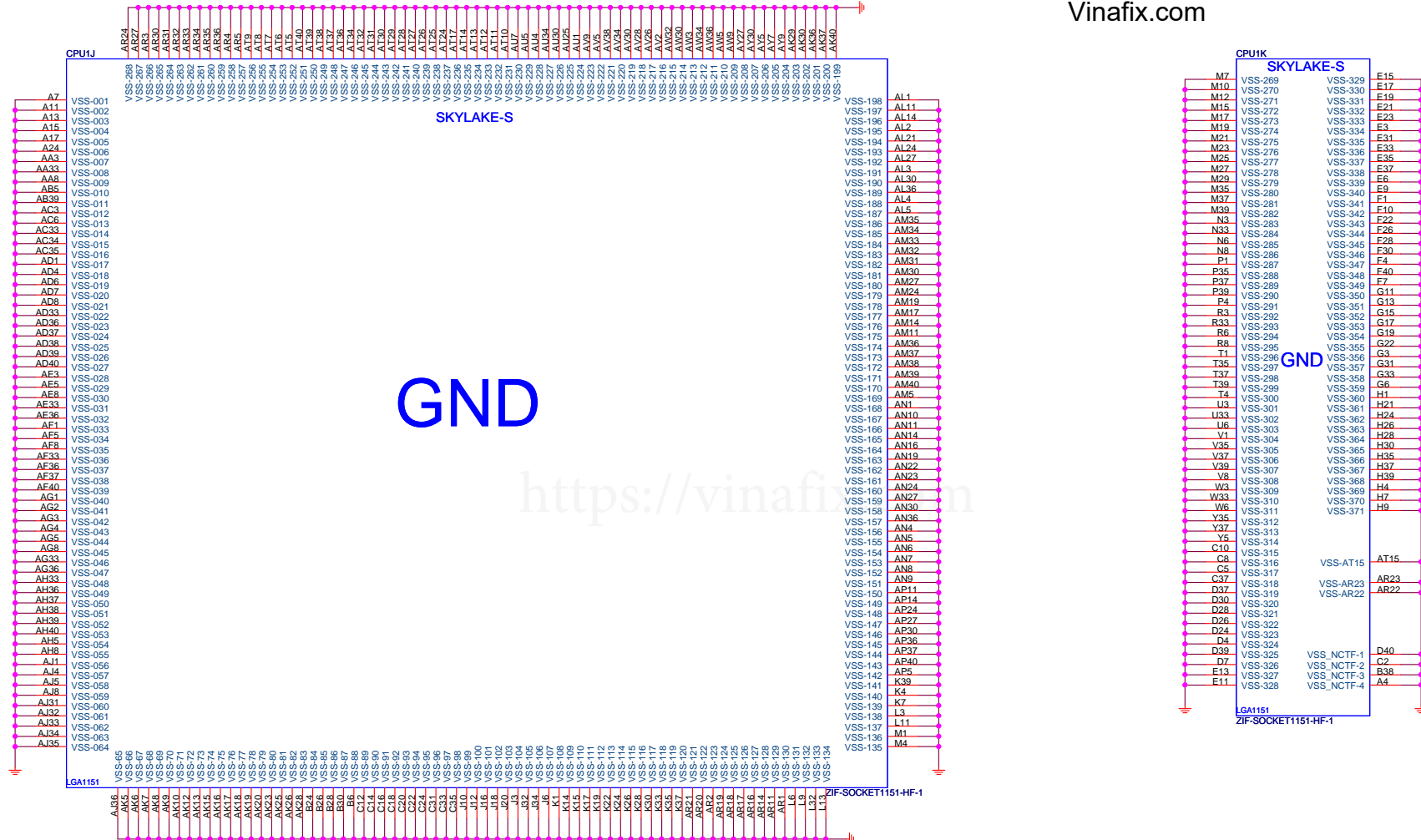
Slot Sequence:
PCIE X16 (By CPU GEN3)





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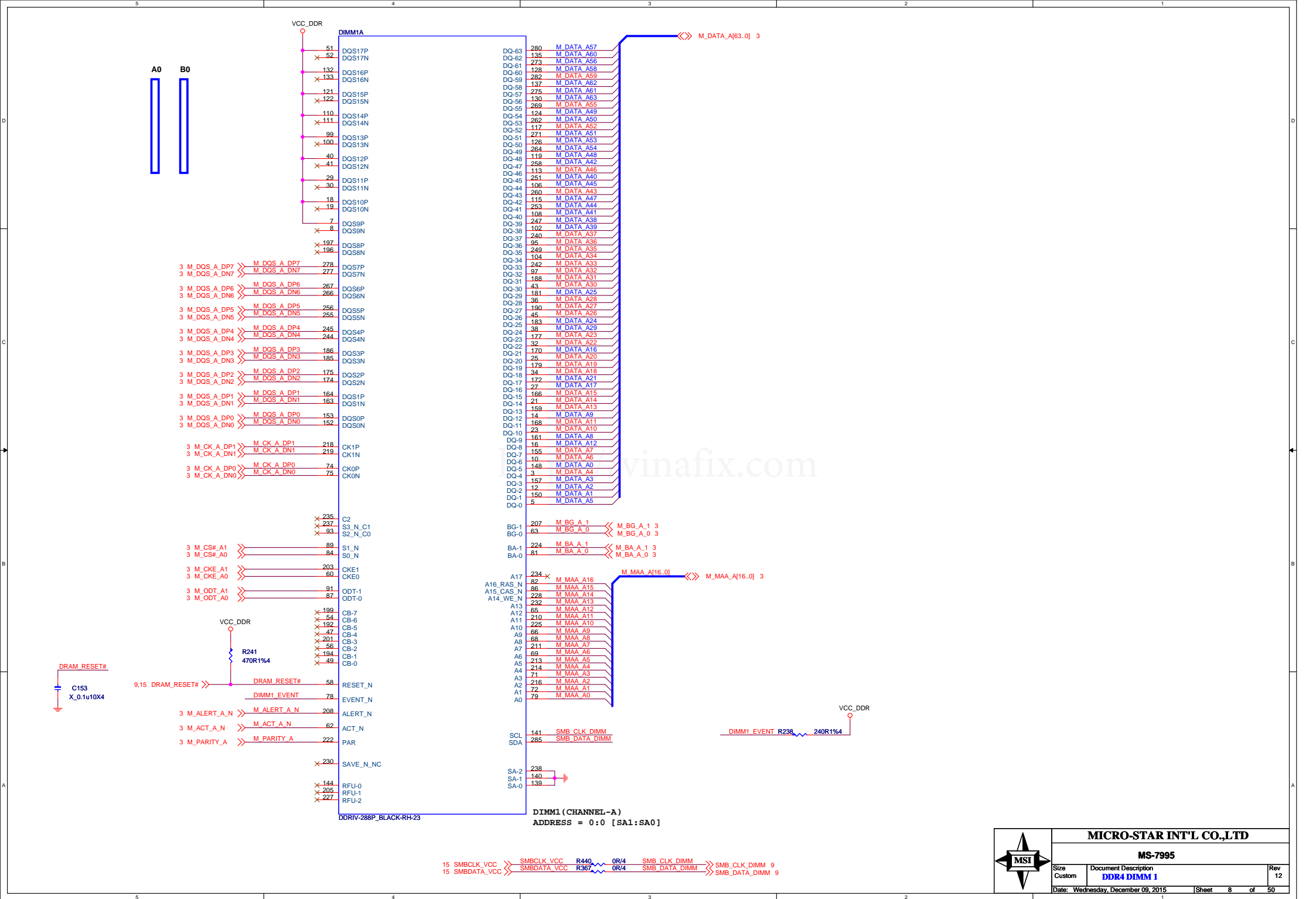


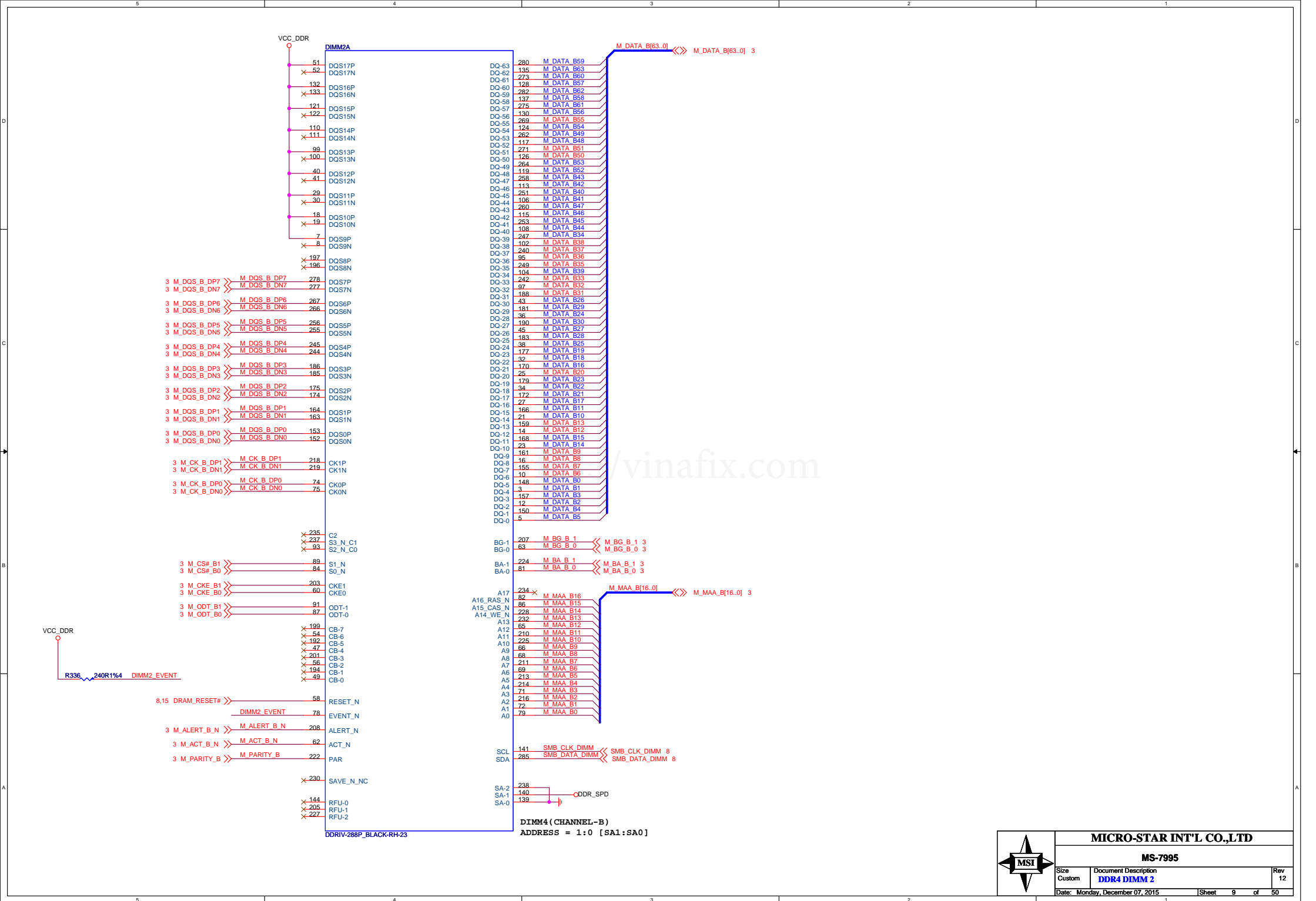


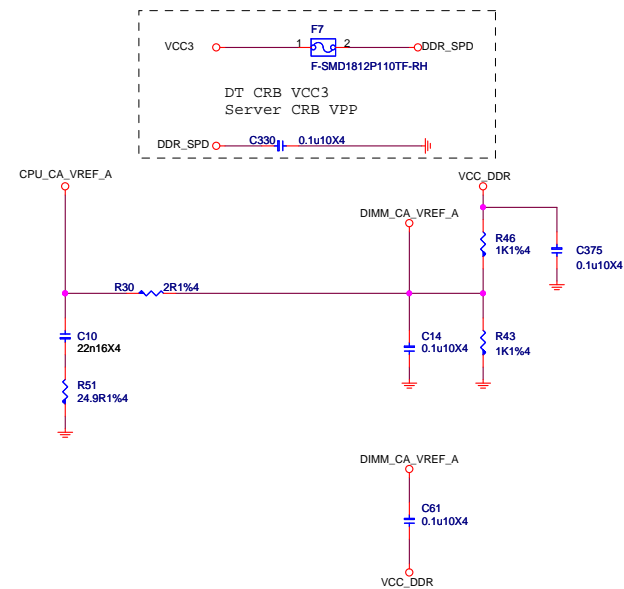
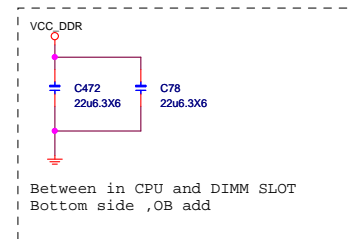
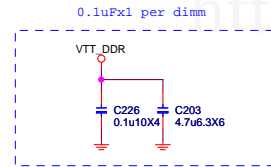
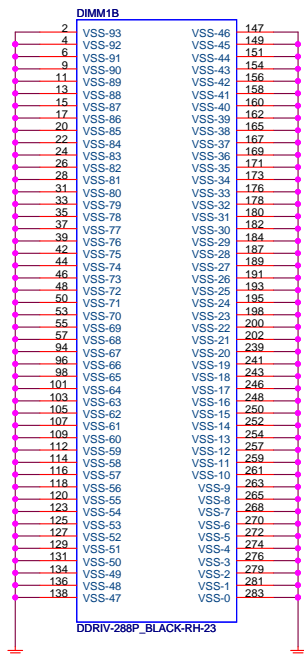
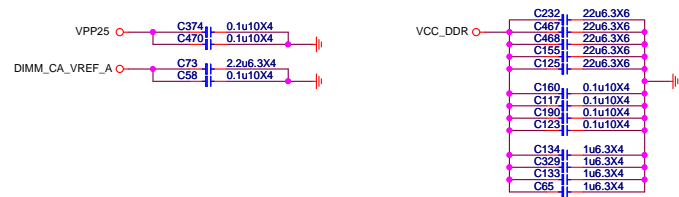
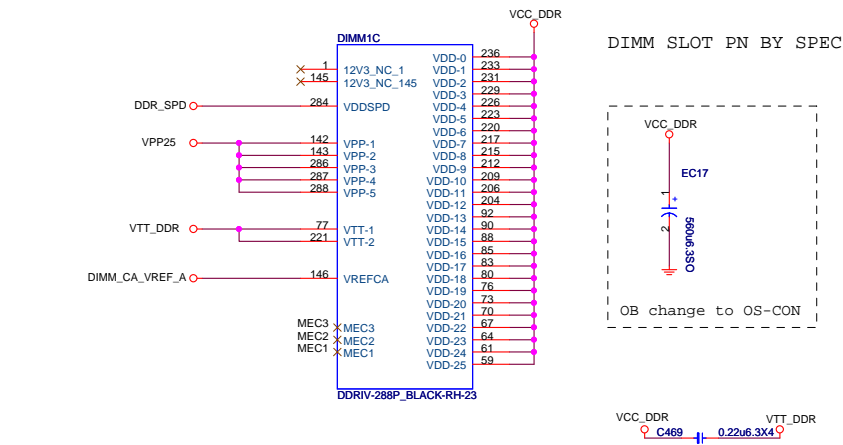
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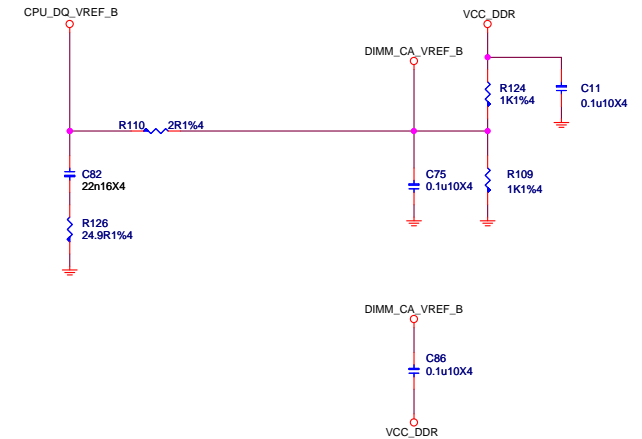
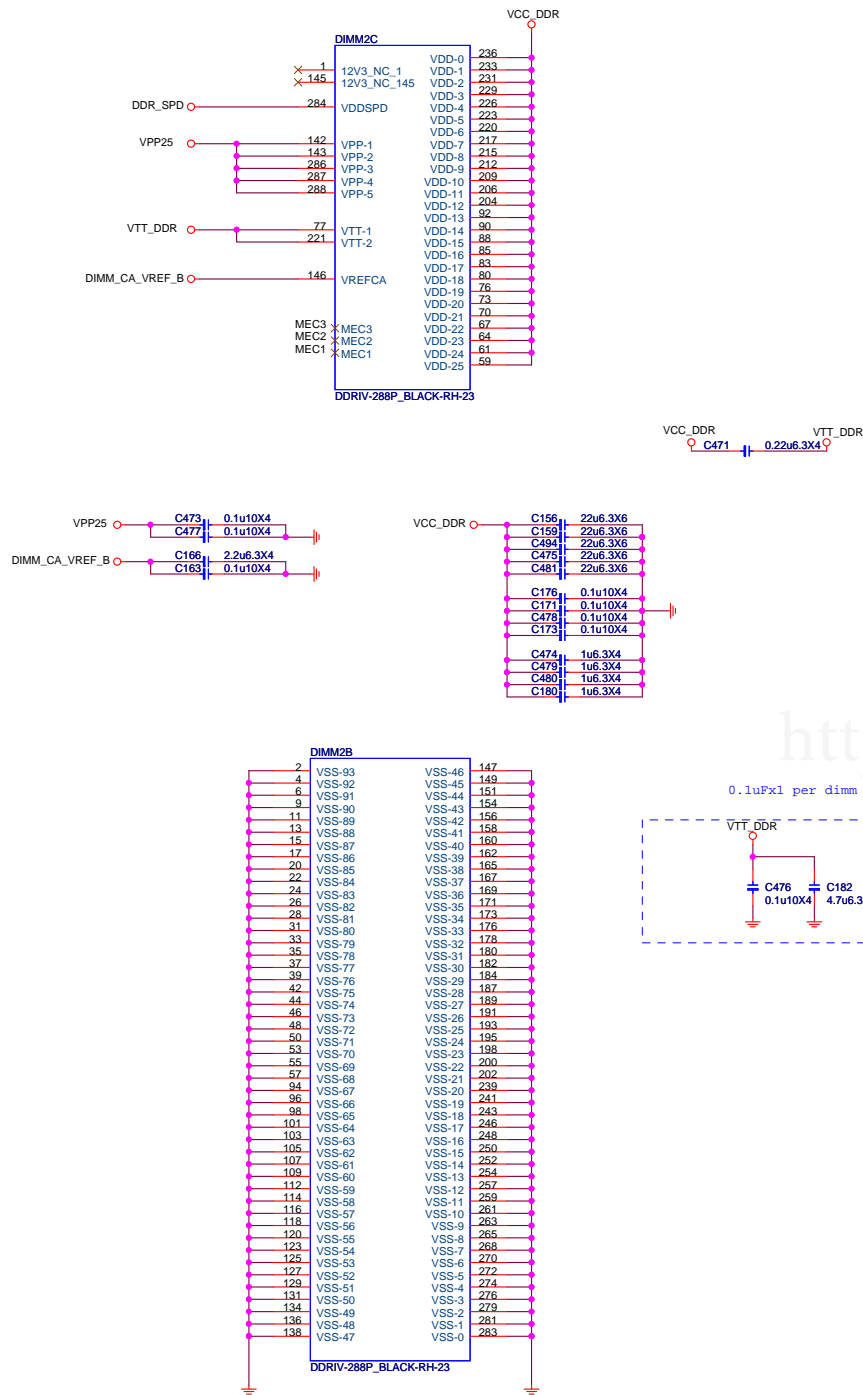
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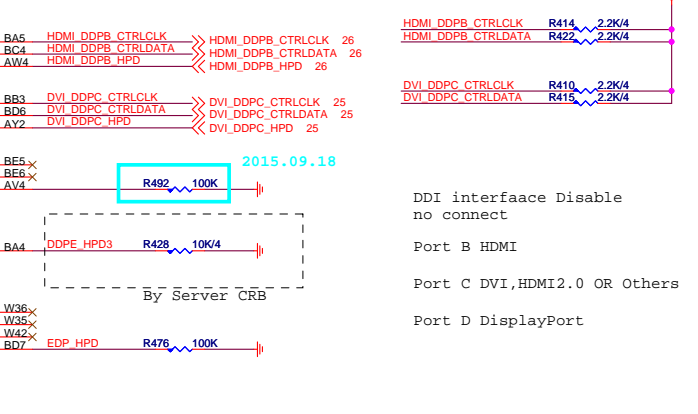
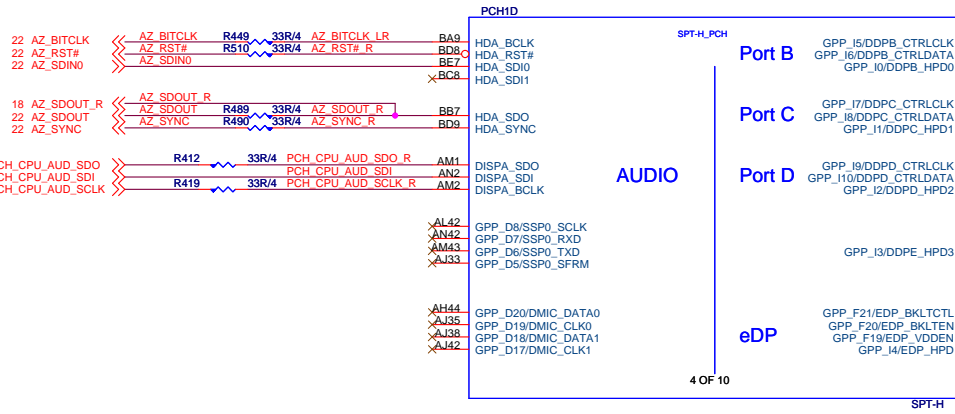
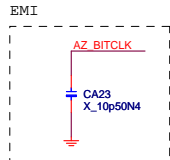




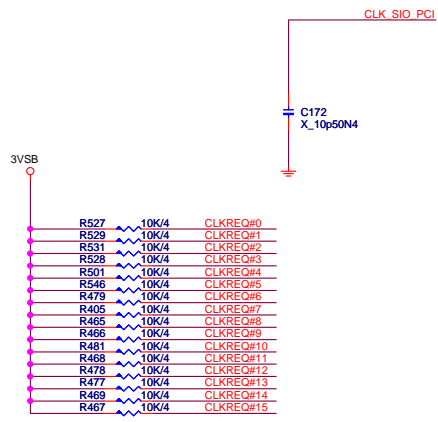




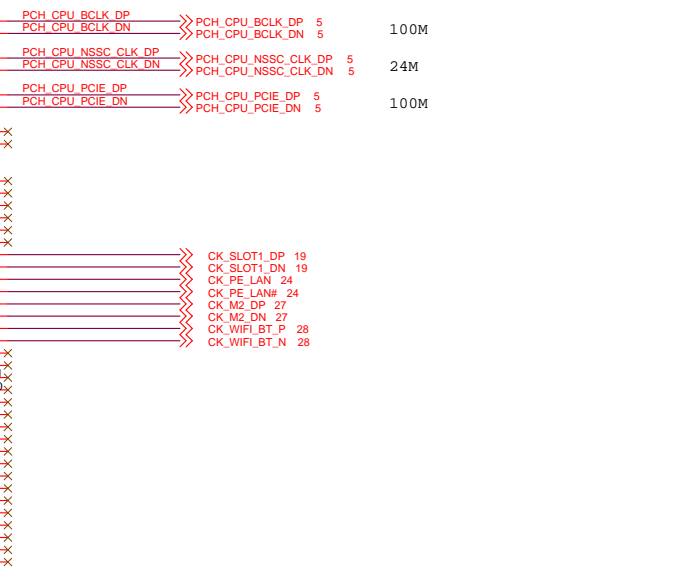
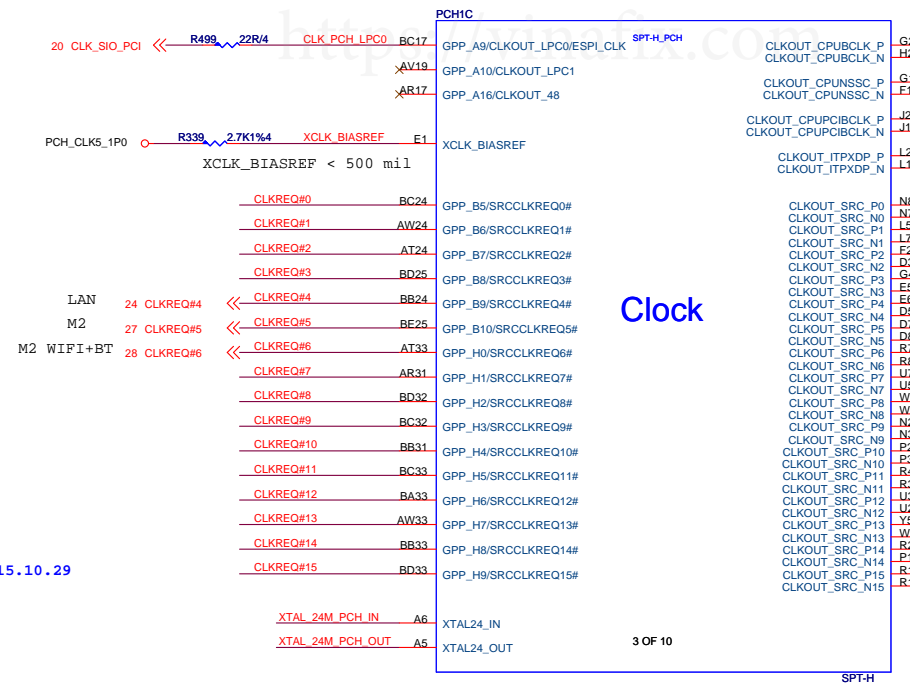
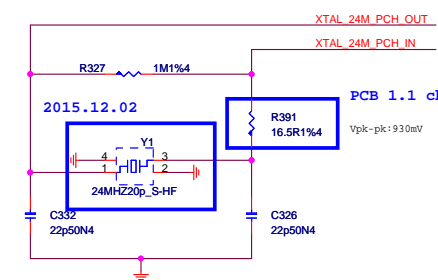
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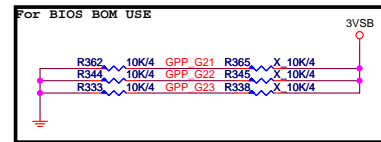
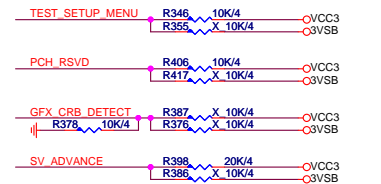
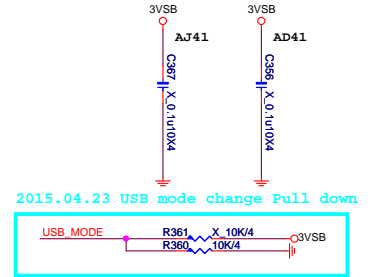
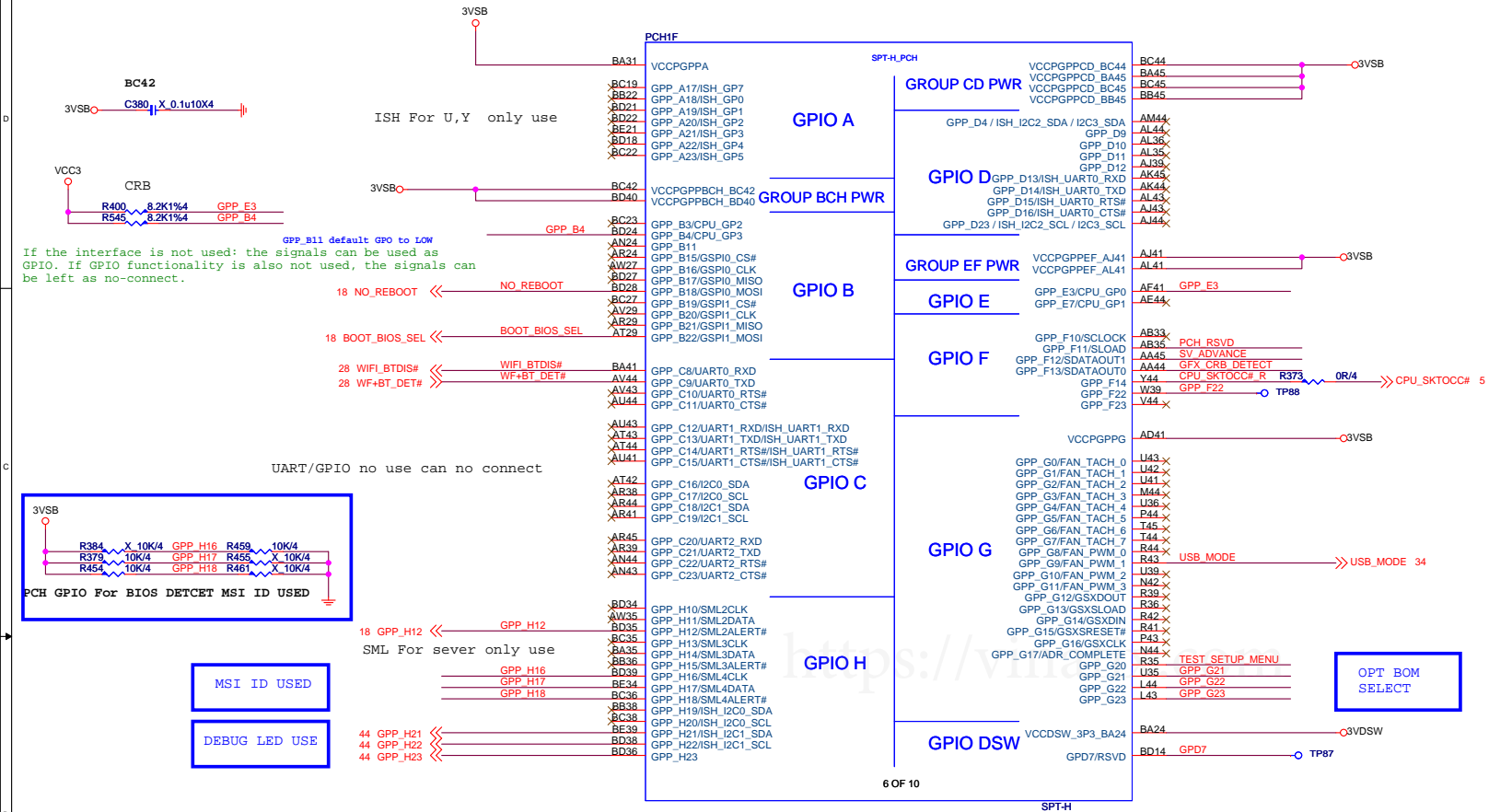


DDI interface Disable
no connect
Port B HDMI
Port C DVI,HDMI2.0 OR Others
Port D DisplayPort



Comtact to SLOT Pin B12
for support L1 PM Substates
ME also can disable this funtion.



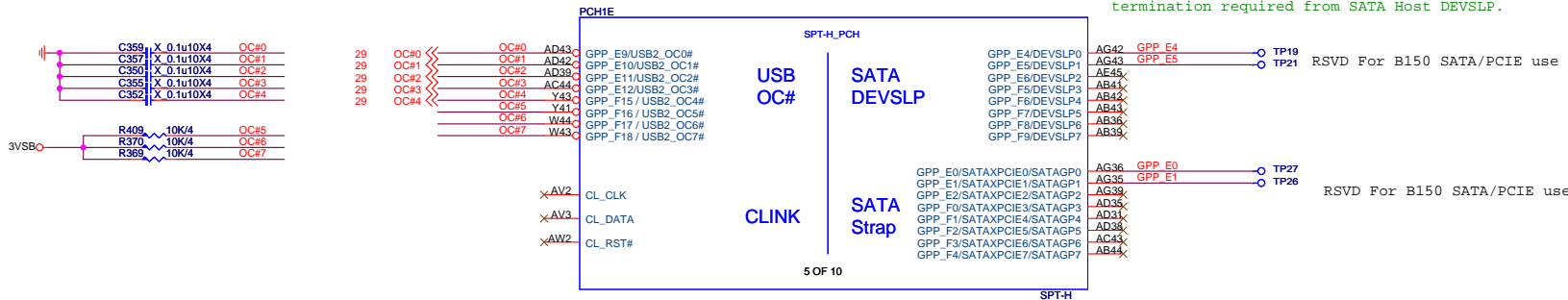


For BIOS BOM USE

	GPP_G21	GPP_G22	GPP_G23
B150 Ac	0	0	0
B150	0	0	1
H170 AC	0	1	0
H110 v1.0	1	0	0
H110	1	1	1

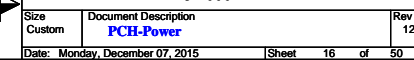
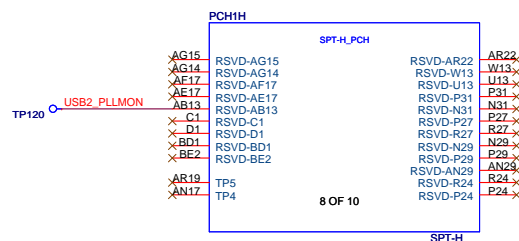
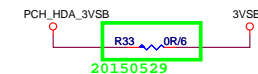
PCH POWER default voltage Diff

When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.



If an AMT capable Intel WLAN device is not implemented then this signal can be left as NO CONNECT (NC).





GND

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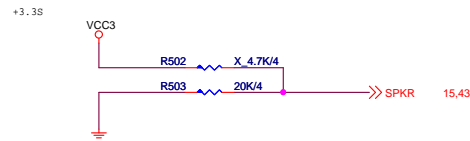


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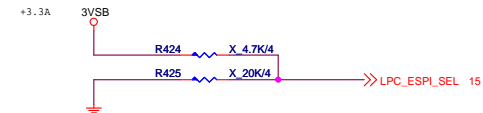
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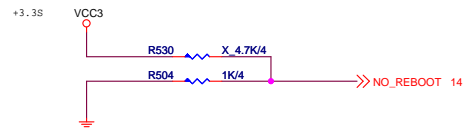


Internal pull-down 20K is disabled after PLTRST#



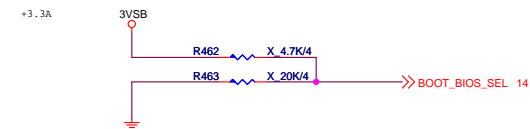
0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMRST



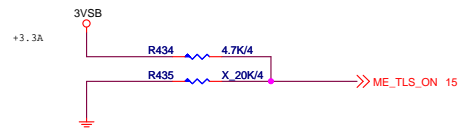
0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#



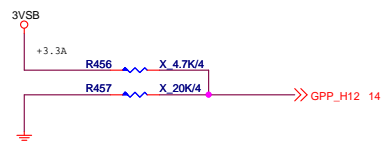
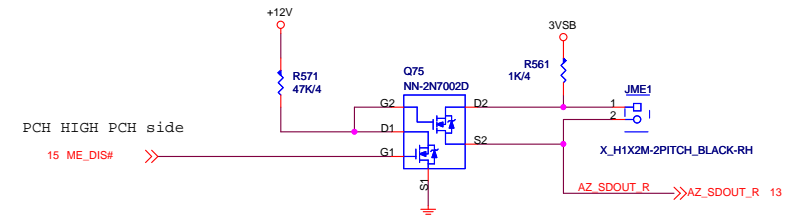
0 : SPI
1 : LPC

Internal pull-down 20K is disabled after PLTRST



0 : DISABLE
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

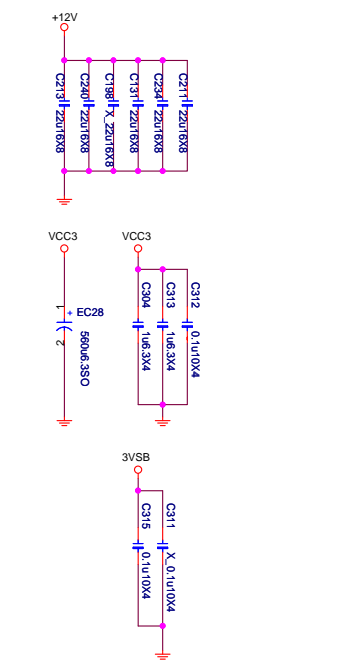
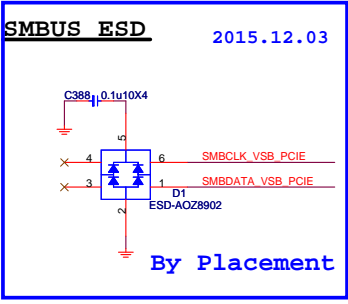
Internal pull-down 20K is disabled after RSMRST



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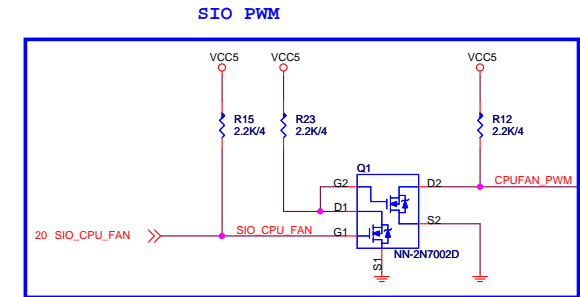
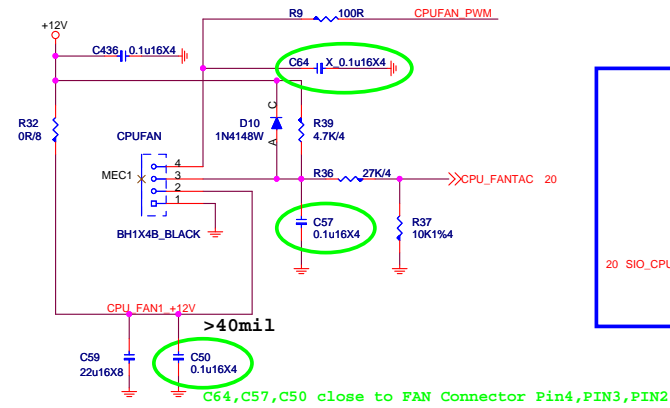
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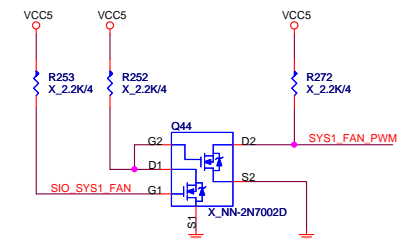
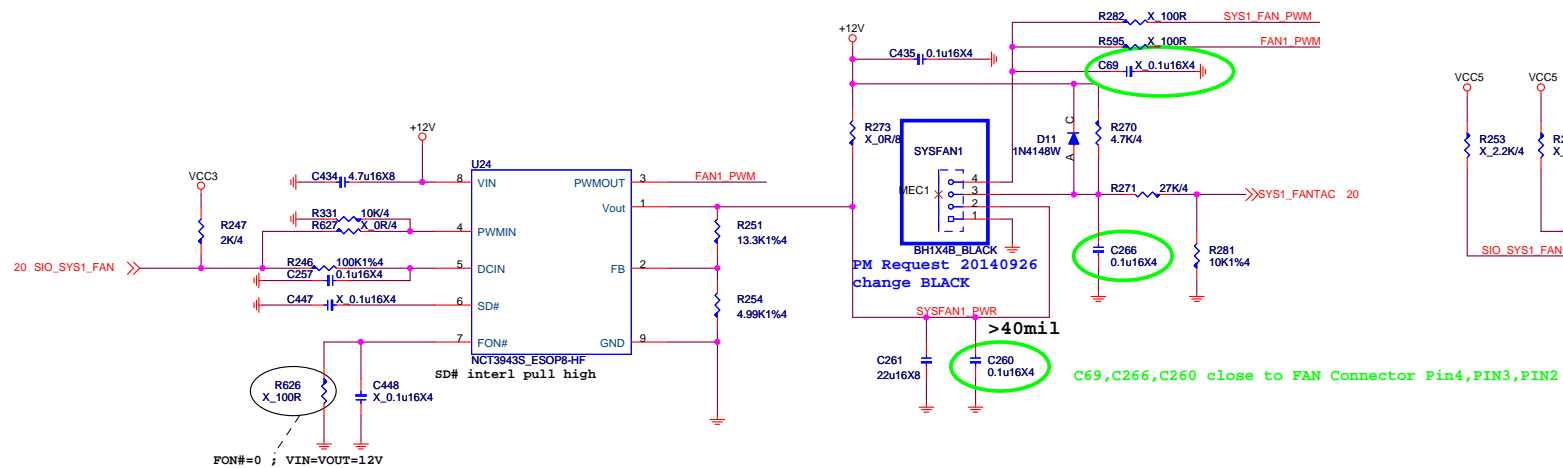


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Type G : 4 PIN CPU FAN FROM SIO



Type H : 4 PIN SYS FAN FROM SIO

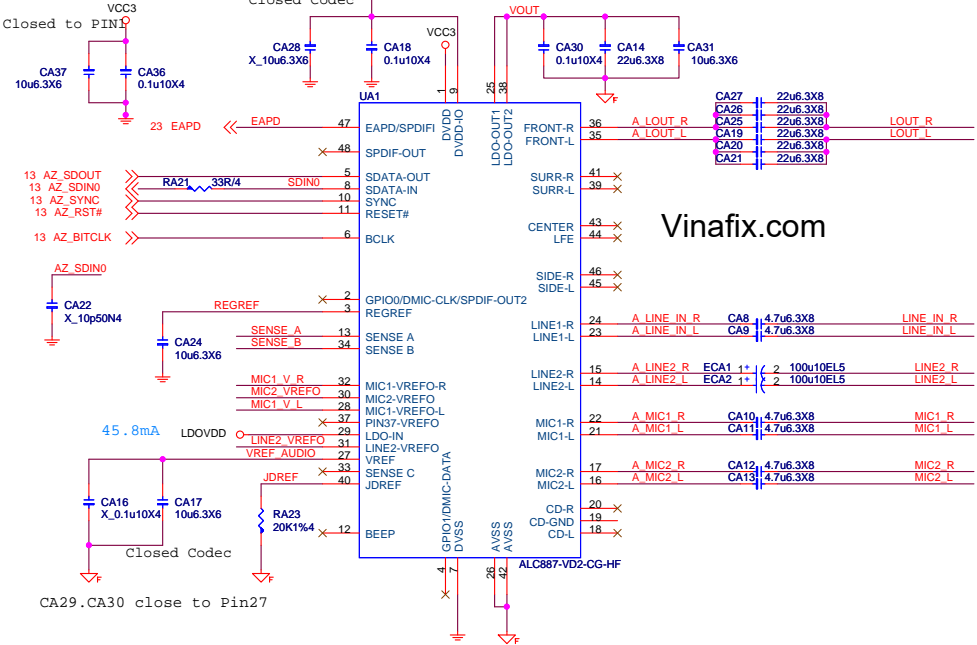


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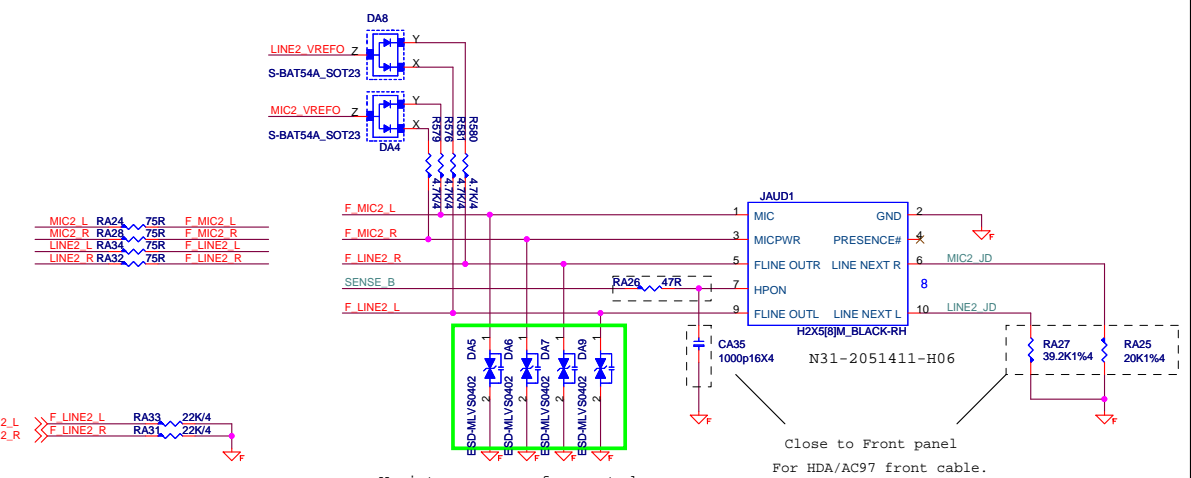
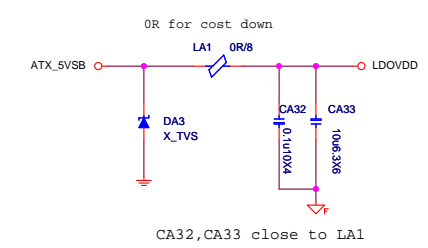
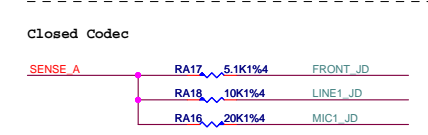
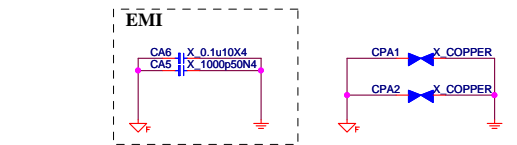
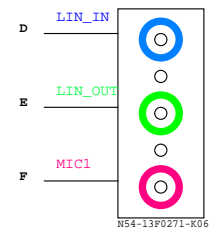
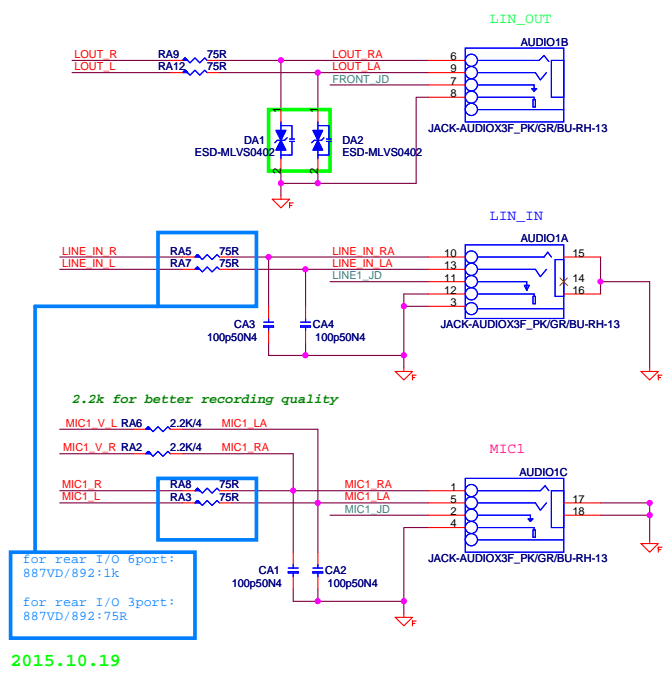
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Type B:
ALC892/887



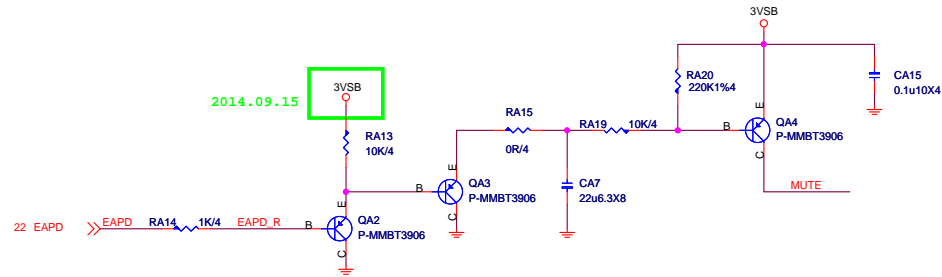
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MSI			
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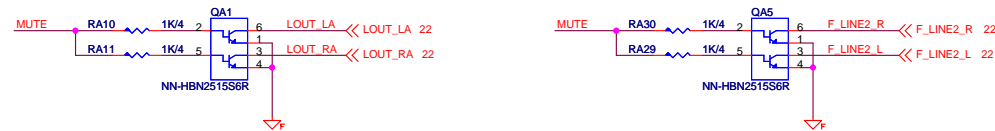
Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog



<https://vinafix.com>

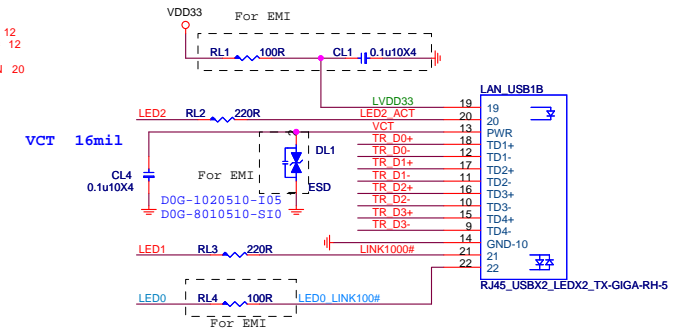
History:

2014/02/13: stuff de-pop circuit of Line out & HP out.

RTL8111G/RTL8111H Giga LAN

8111H:B06-08111CC-R09
8111G:B06-081116C-R09

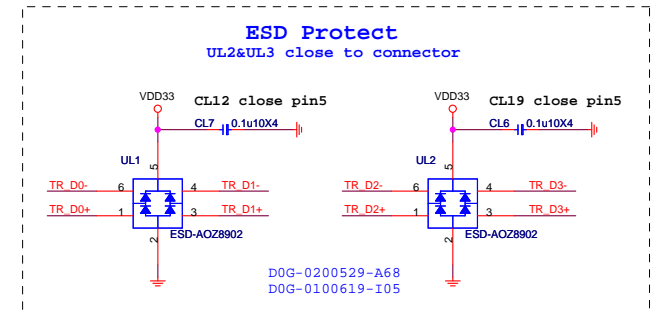
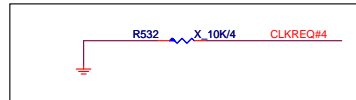
LAN Connector



Pin33: 4 via from top layer to GND layer and make the via at the center of IC.

<https://vinafix.com>

For module unstuff



8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

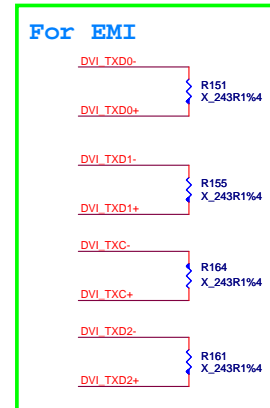
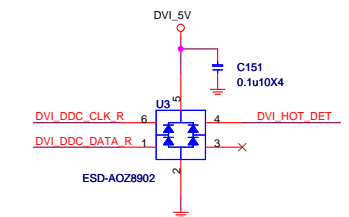
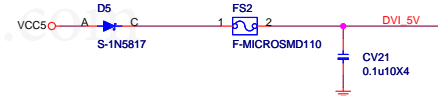
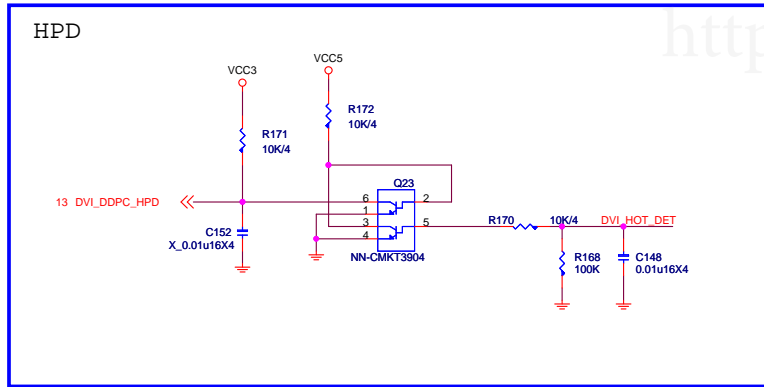
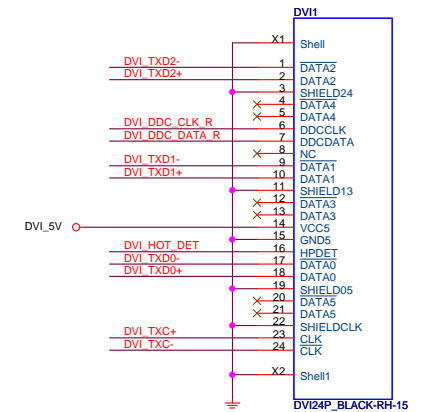
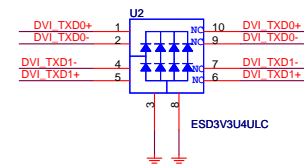
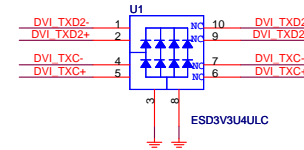
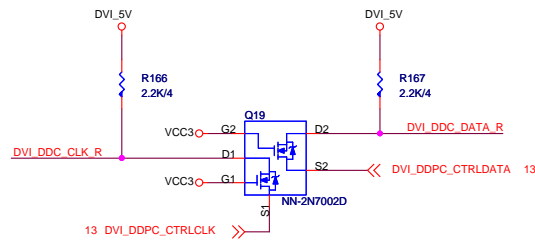
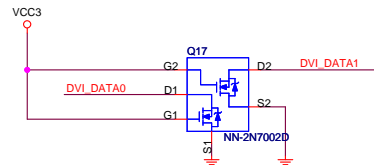
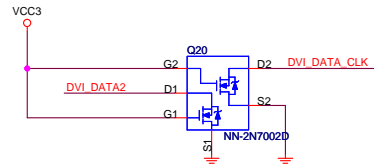
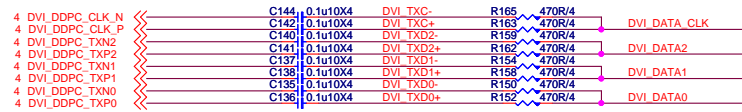


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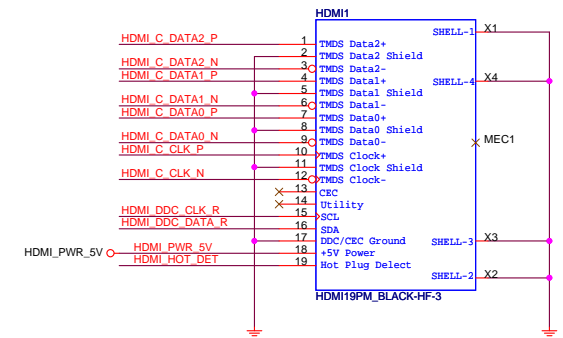
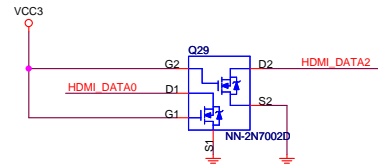
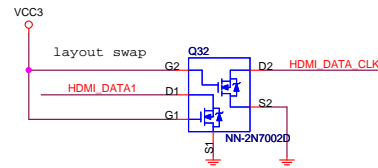
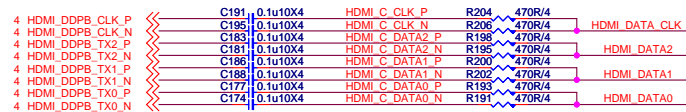
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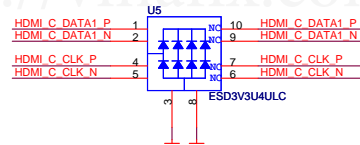
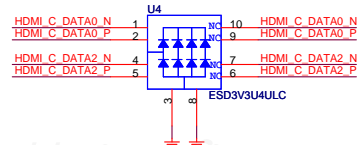
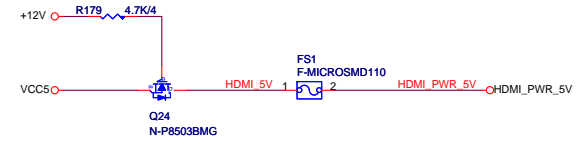
DVI max resolution is 1920x1200 @ 60 Hz



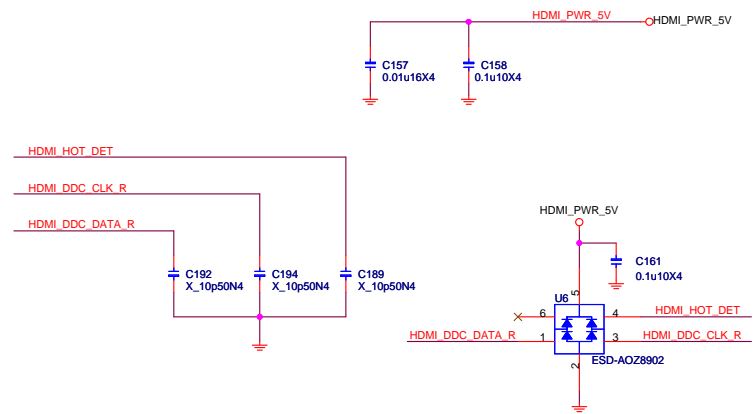
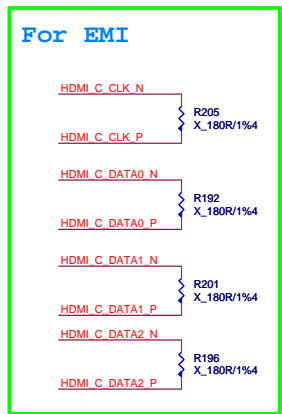
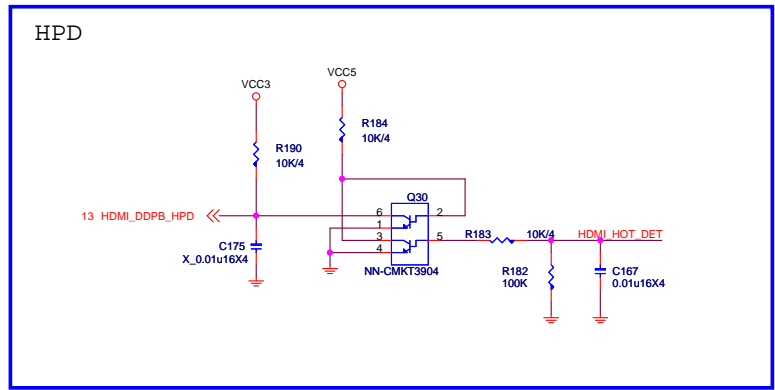
The HDMI* interface supports HDMI with 3D, 4Kx2K@24Hz, Deep Color, and x.v.Color.

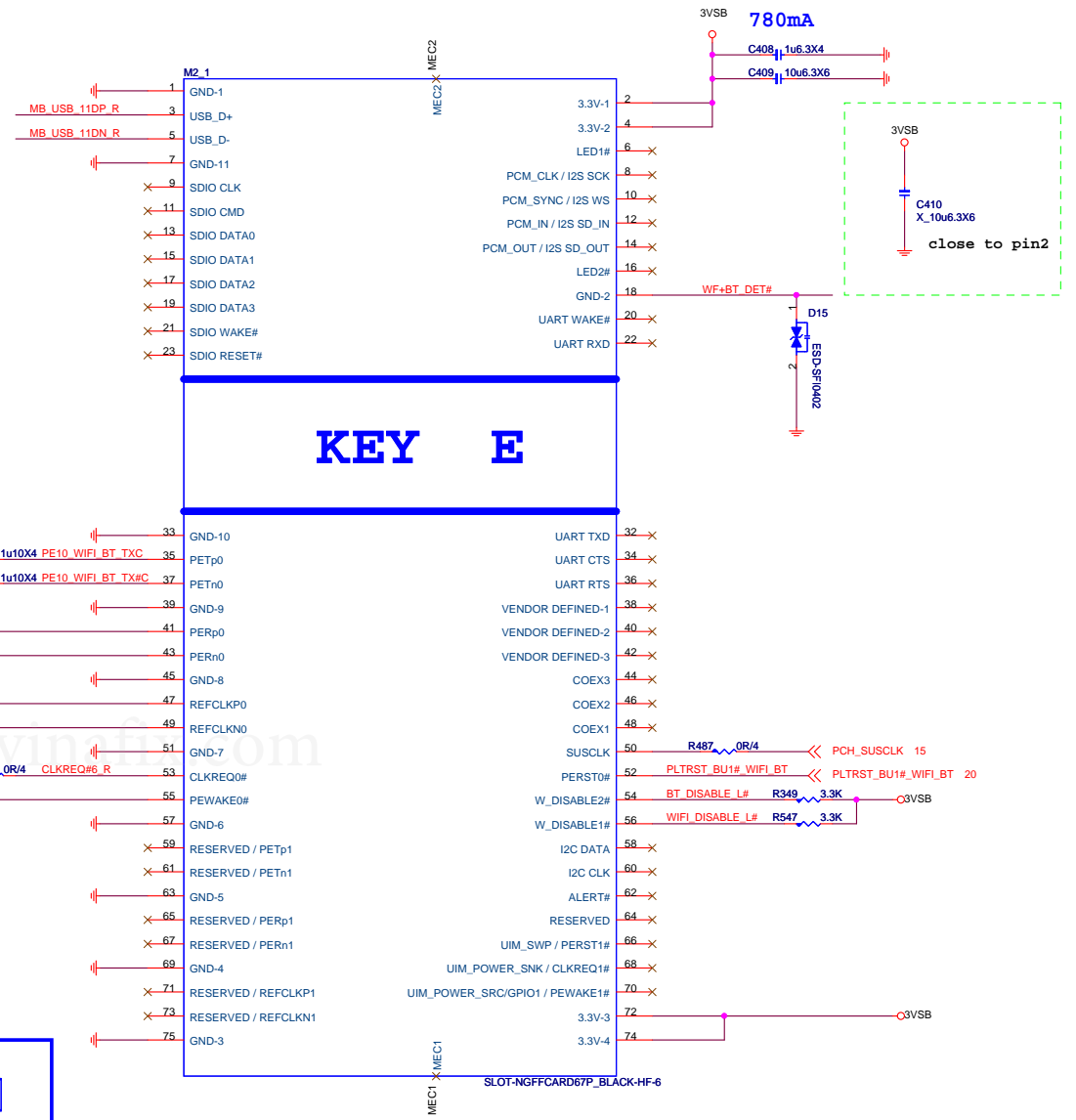
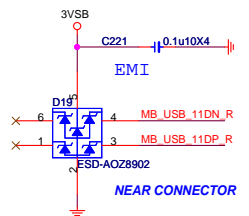
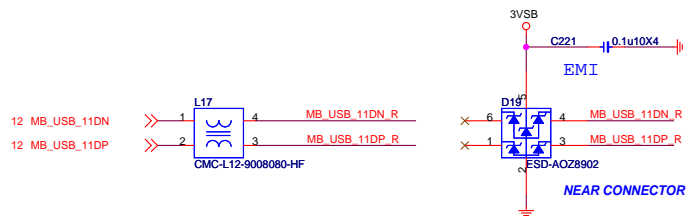
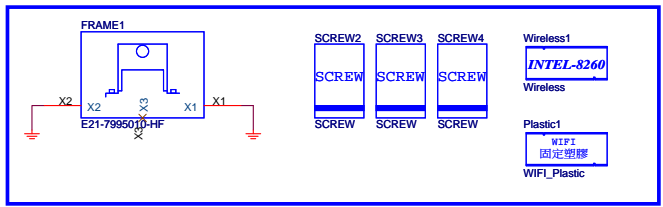
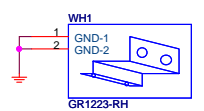
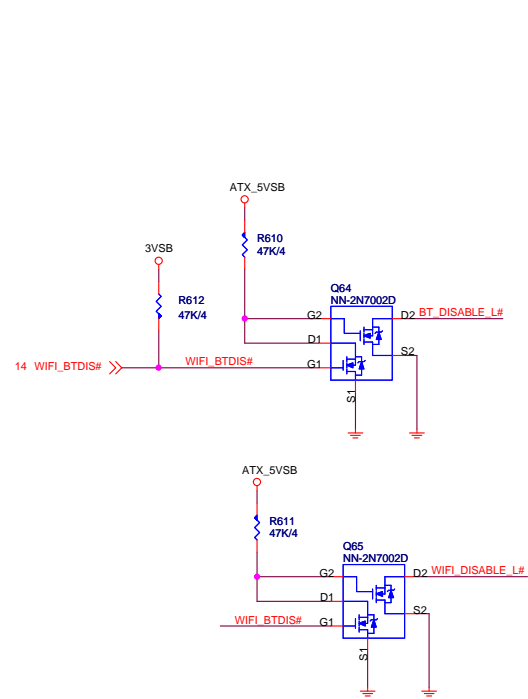


Vinafix.com

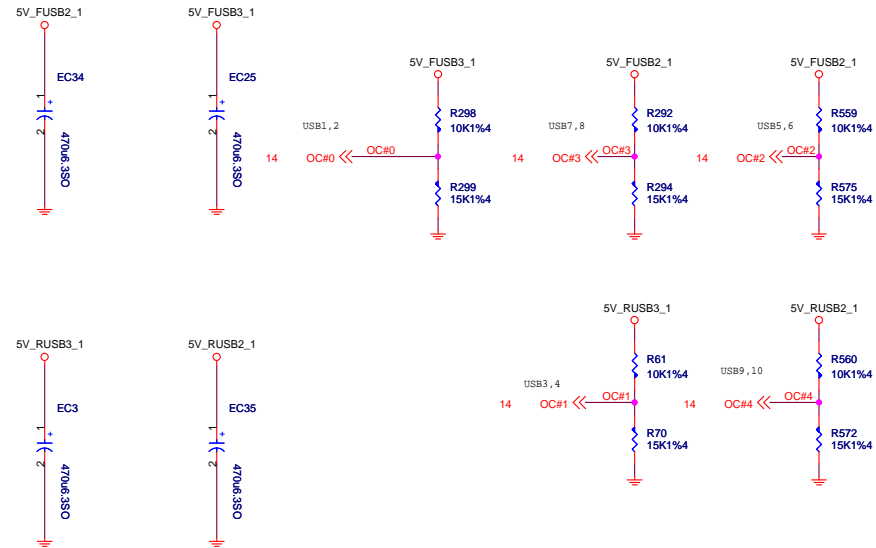
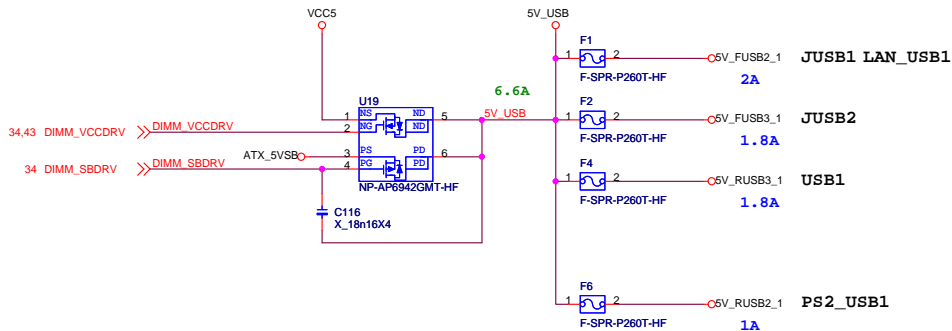


<https://vinafix.com>



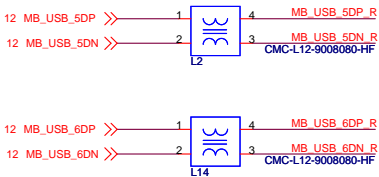


USB POWER

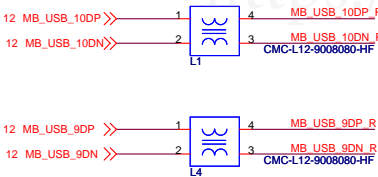


Vinafix.com

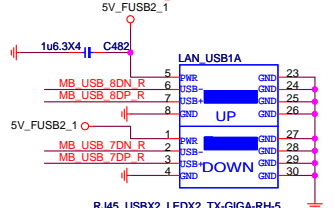
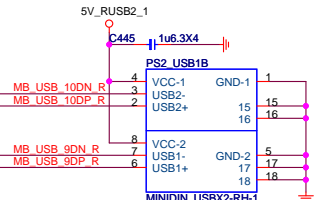
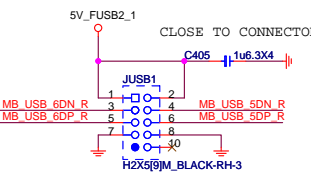
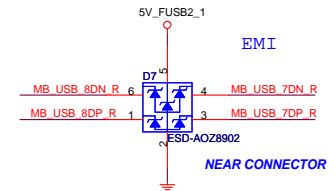
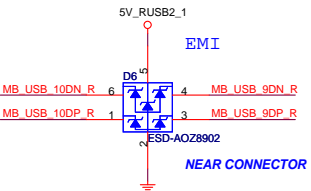
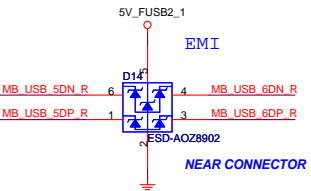
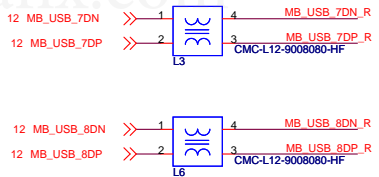
FRONT USB PORT 5,6



FRONT USB PORT 9,10



FRONT USB PORT 7,8

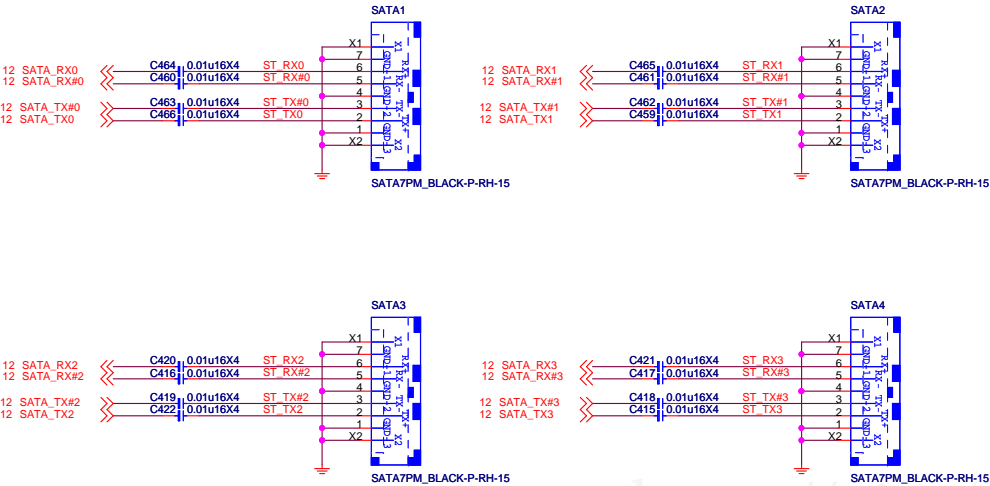


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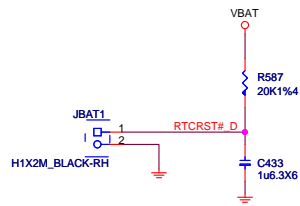
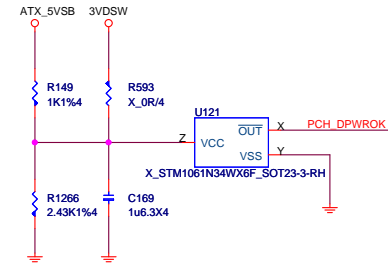
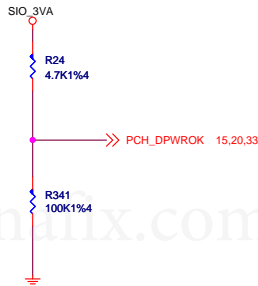
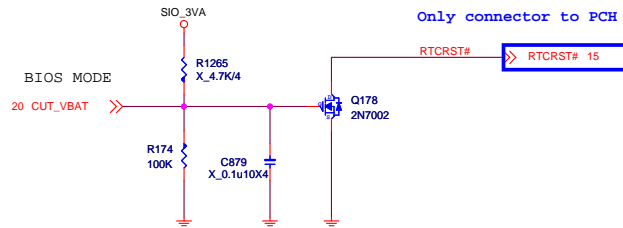
MS-7995

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SATA GEN3



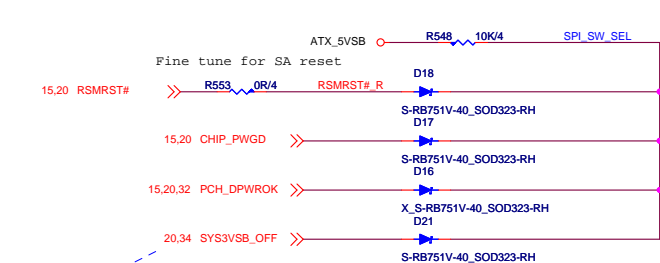
<https://vinafix.com>



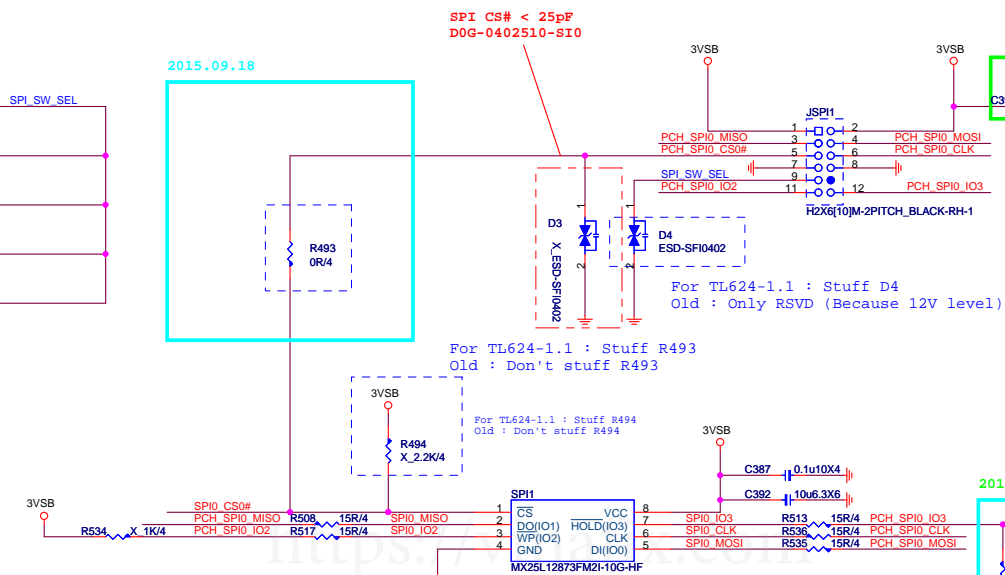
RTCRST# R588 X_0R/4 RTCRST#_D

co-lay

15 PCH_SPI0_MOSI << PCH_SPI0_MOSI
15 PCH_SPI0_MISO << PCH_SPI0_MISO
15 PCH_SPI0_CLK << PCH_SPI0_CLK
15 PCH_SPI0_CS0# << PCH_SPI0_CS0#
15 PCH_SPI0_IO2 << PCH_SPI0_IO2
15 PCH_SPI0_IO3 << PCH_SPI0_IO3



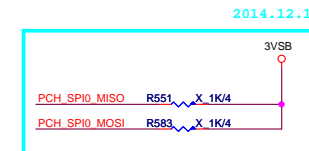
For TL624-1.1 (SKYLAKE)
In skylake,PCH core is powered by VSB which need sink RSMRST# to low by SPI_SW_SEL.



2014.08.25

Close to JSP11

C399 0.1u10X4



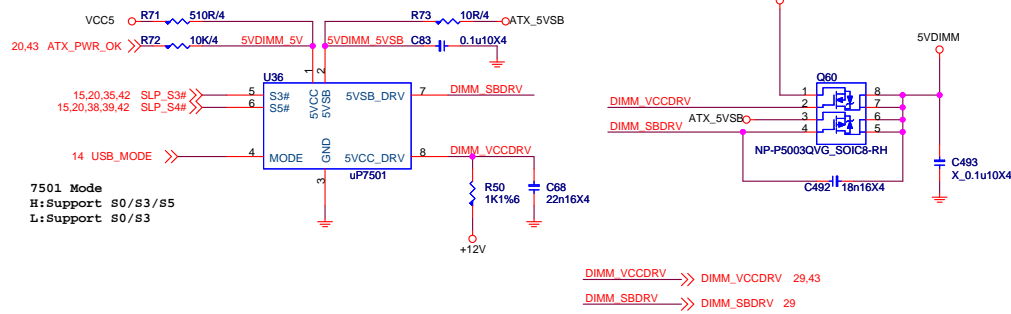
- * if you not support Standby power in S5 Status, component Q14.G Pull-high to +12V & Q14 MOS select 2N7002
 - * if you support Standby power in S5 Status(Ex; PCH is B75 Chipset), component Q14.G Pull-high to ATX_5VSB, Q14 must select "Vth" under 1V (Component Suggestion as below)
- D03-0341409-A68 / D03-0230019-A30

2014.09.24 For intel MOW36 update
pull down resistor on SPI0_IO3 is needed for SKL S/H platforms with pre-ES1/ES1 ES2 samples.
20150115
update this issue for PRE-ES2/ES2 refer mail 20150115
From syng

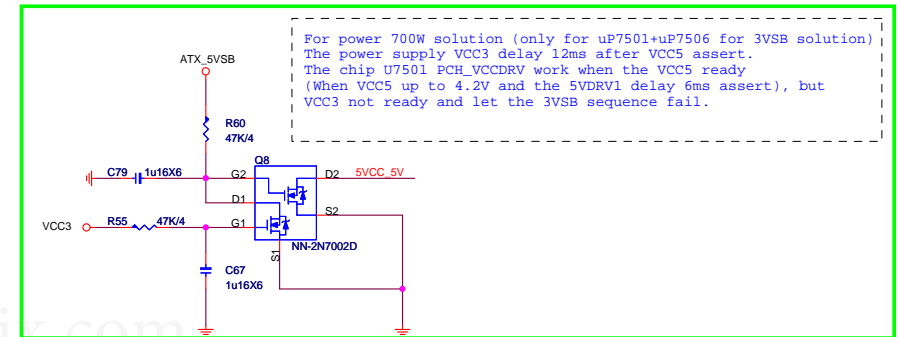
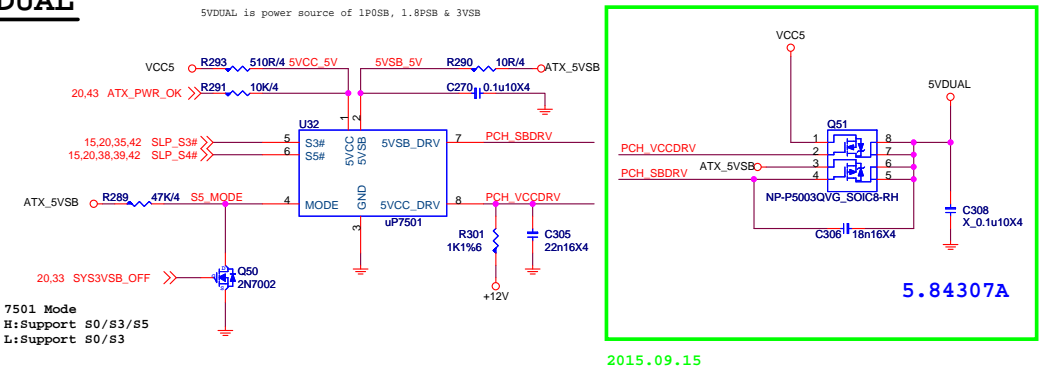


MICRO-STAR INT'L CO.,LTD		
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Size Custom	Document Description BIOS ROM	Rev 12
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5VDIMM FOR DDR

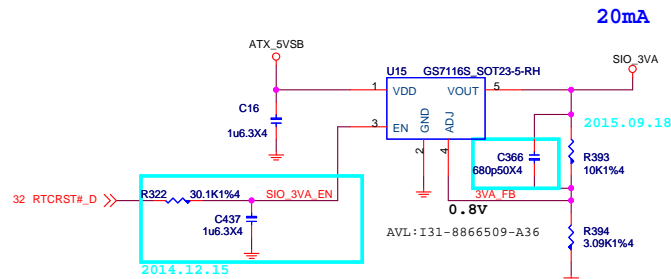


5VDUAL

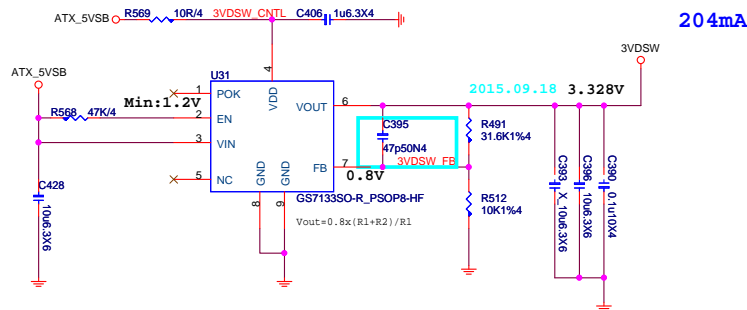


<https://vinafix.com>

SIO_3VA

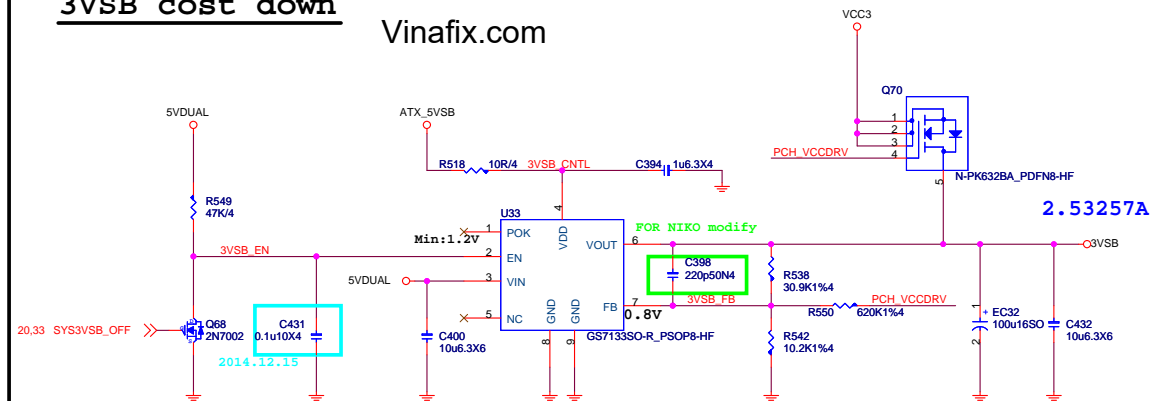


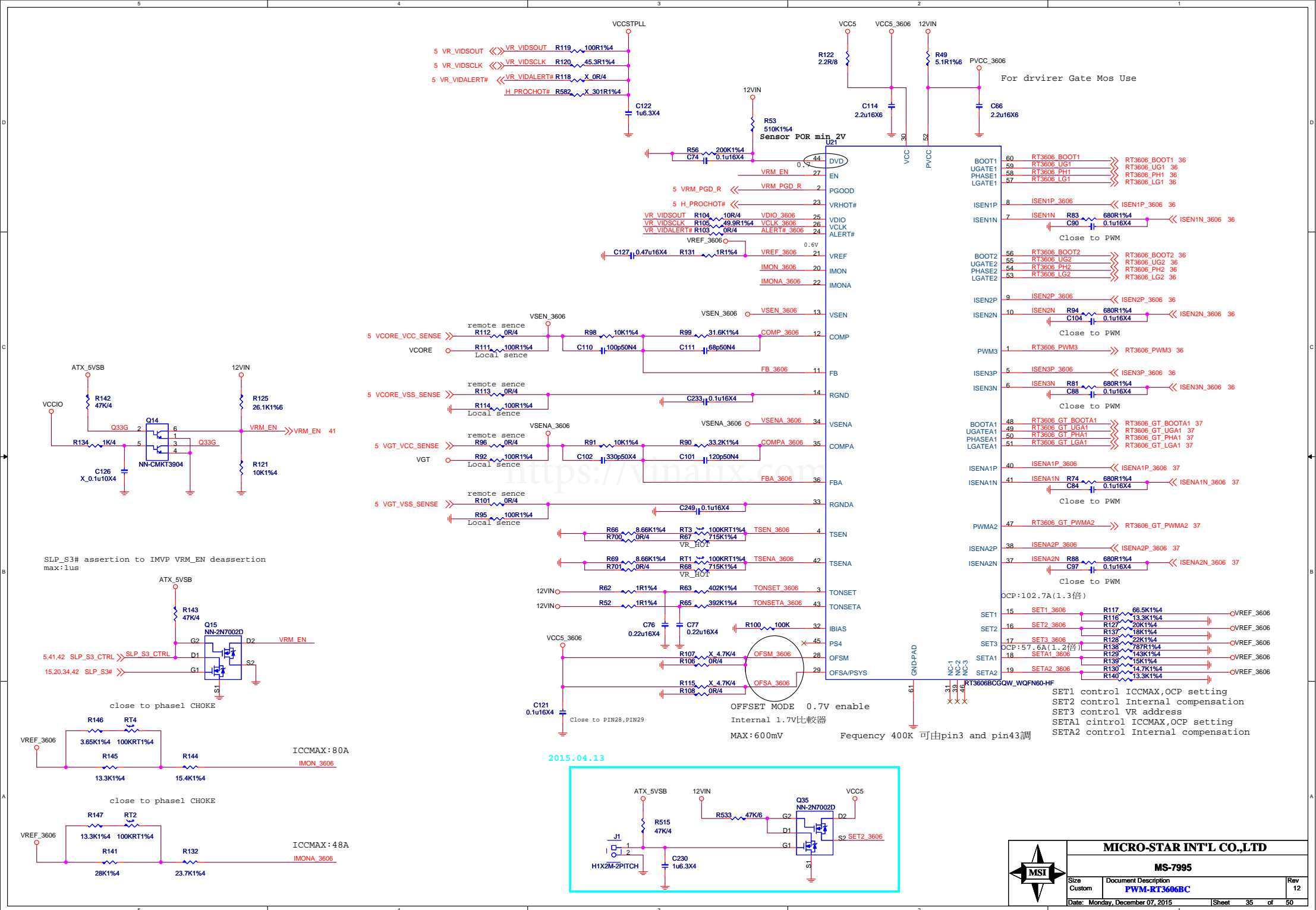
3VDSW

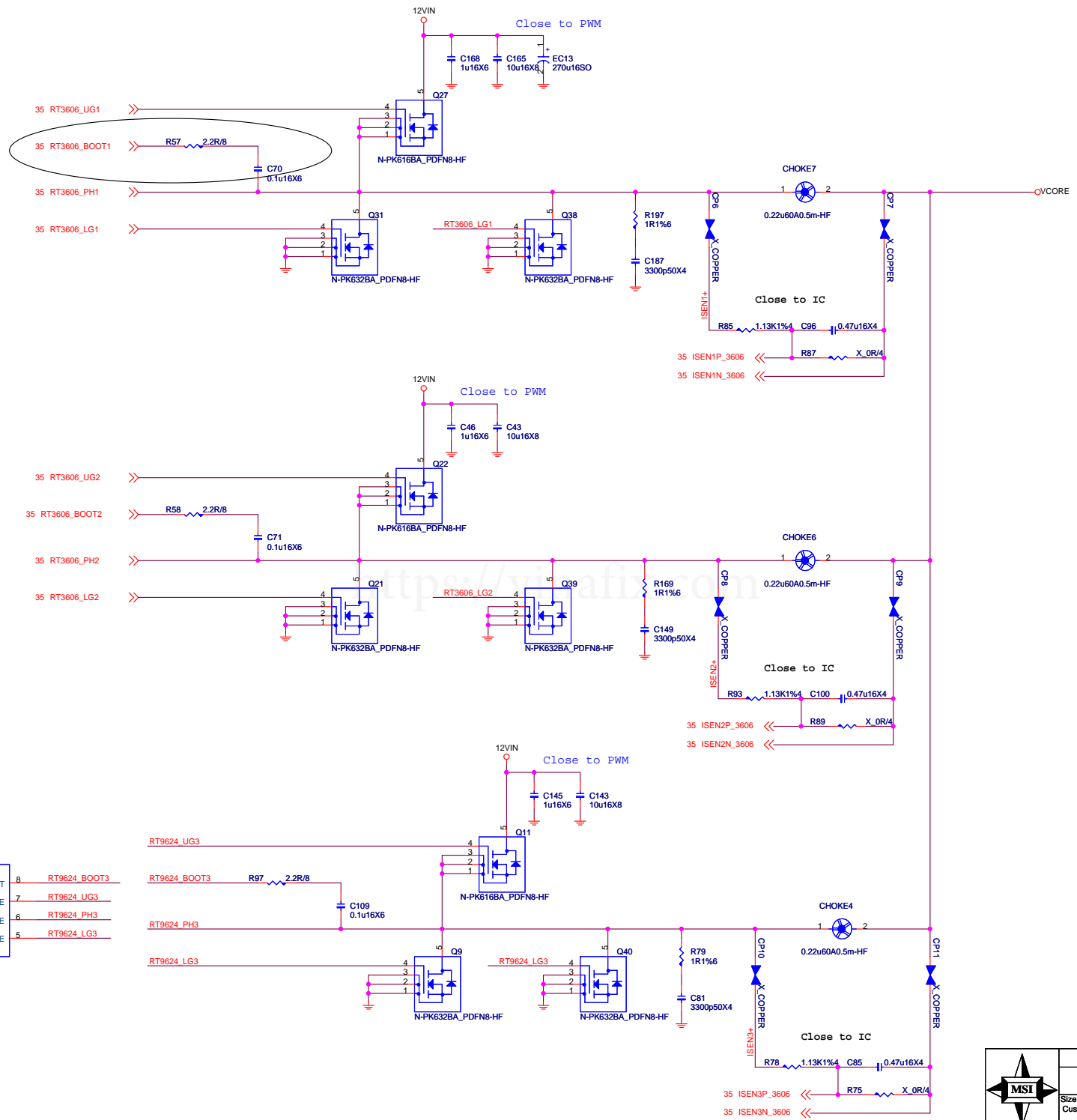


3VSB cost down

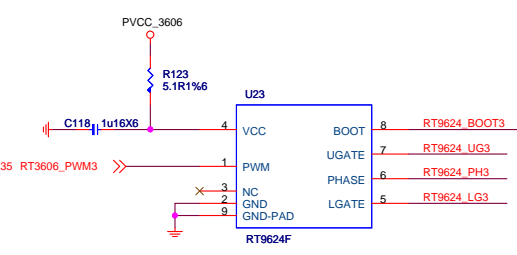
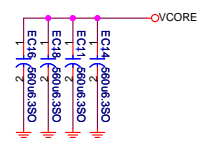
Vinafix.com








ICCMAX: 79A
LL: 2.1m ohm



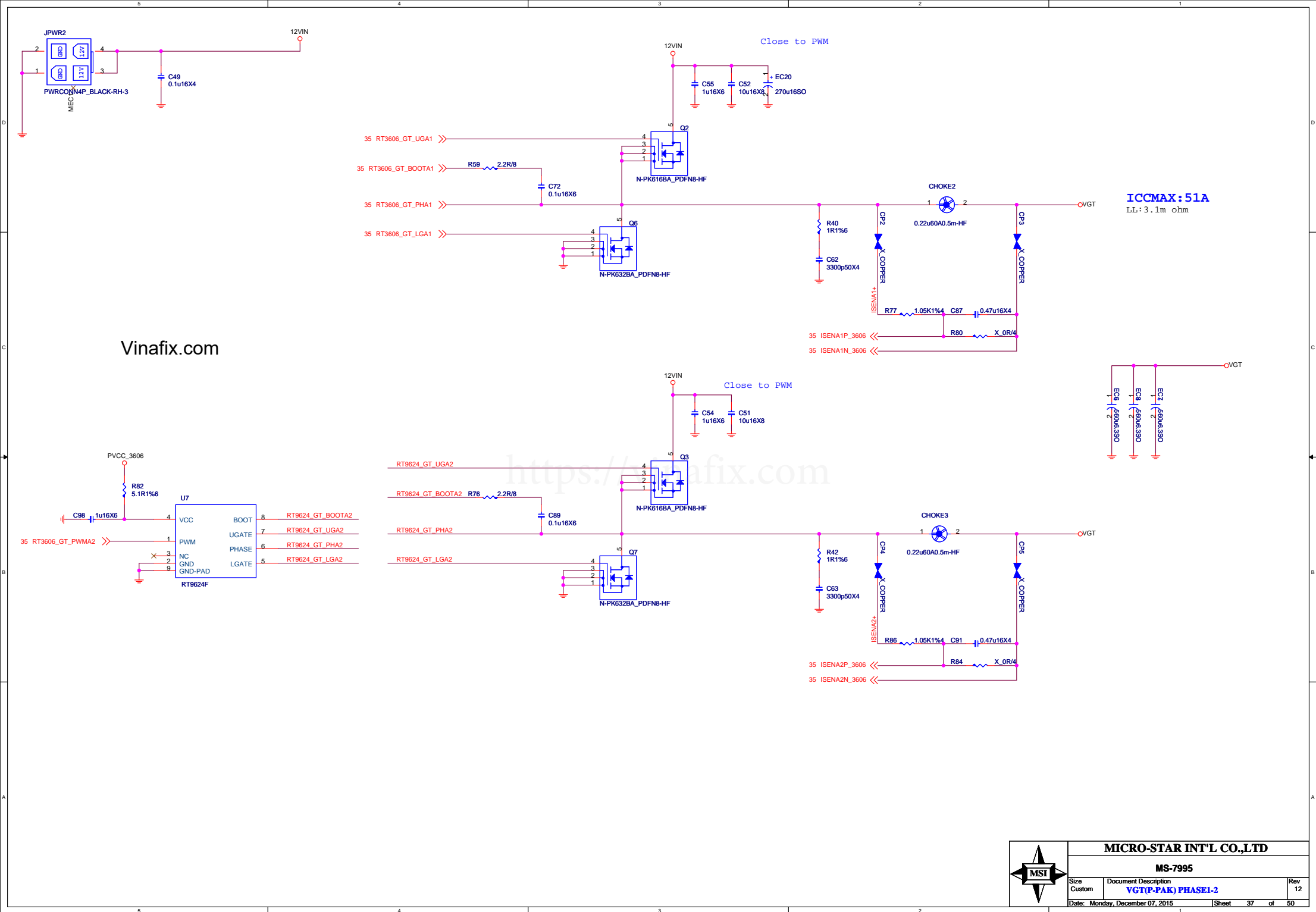


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Size	Document Description	Rev
Custom	VCORE(P-PAK) PHASE1-3	12

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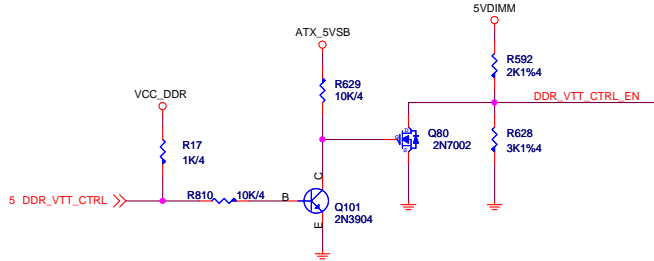
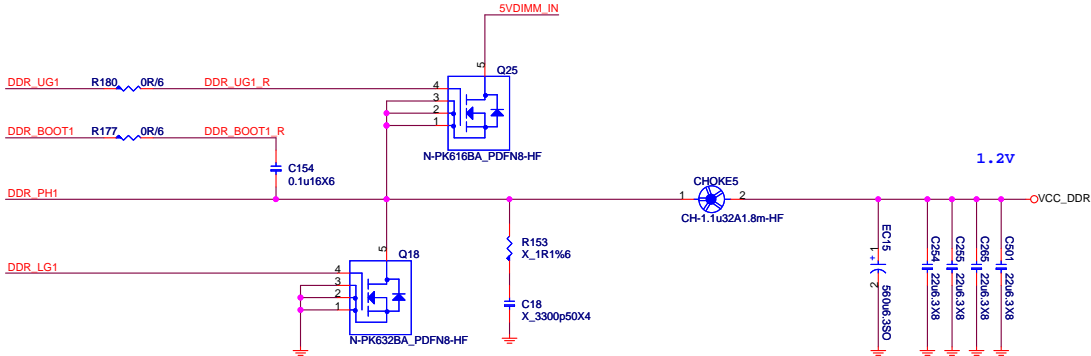
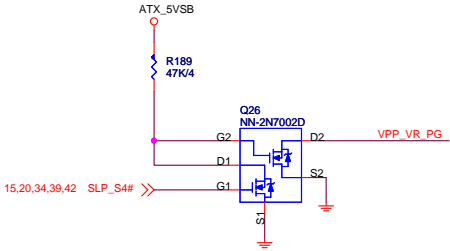
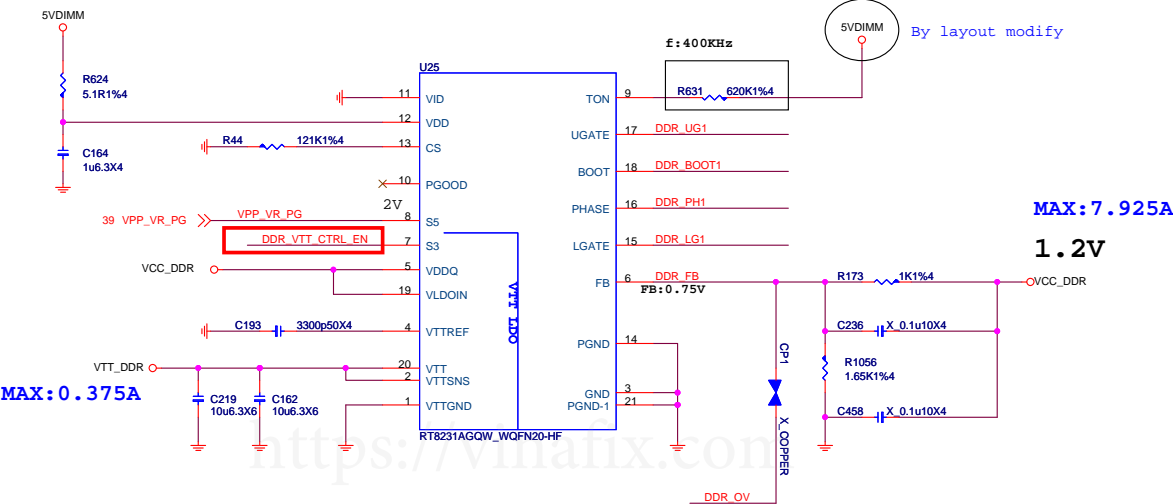
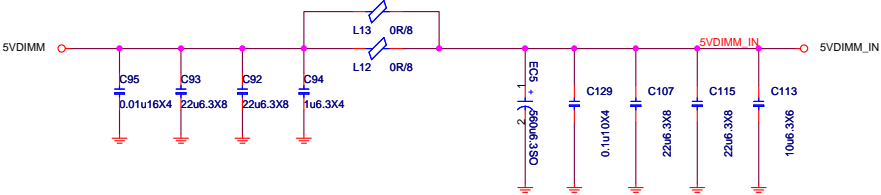
ICCMAX: 51A
LL: 3.1m ohm

DDR4_1.2V 2.8A+ 4.75A+0.375A=7.925

2.8A FOR CPU
9.5A FOR 4DIMM DDR4
4.75A FOR 2DIMM DDR4
0.375A FOR VTT_DDR

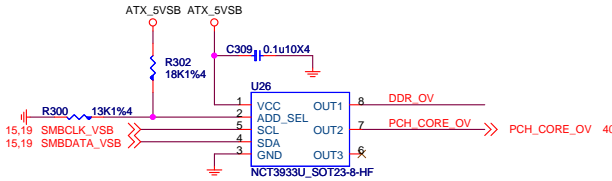
OCP = 7.925A*1.5=11.8875A
Rlimit(R44)
Current Limit =121K*5uA/10/5mohm
--> 121Kohm(12.1A)

$$I_{rms} = I_{out} * \sqrt{((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))}$$
$$= 9.357 * 0.44$$
$$= 4.154A$$



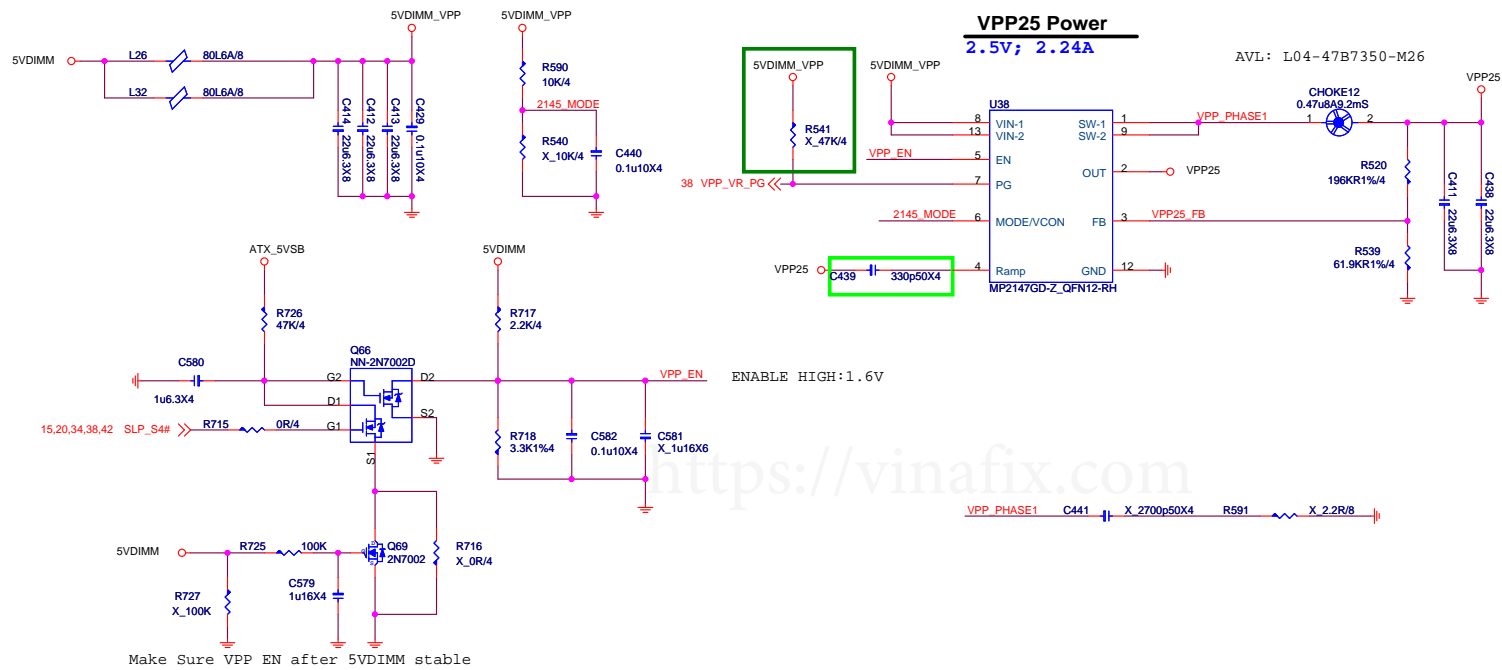
UPI VOLTAGE CONSOLE

0x26 : RH=18K, RL=13K



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2DIMM :1.12A FOR DDR VPP2.5V



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PCH 1VSB

1.0V; 9.142A+5.5A=14.642A
(6.54A + 0.132*4+0.154*6+0.054+0.132*3)

OCP = 21.963A

Rocset = 1.5 * I_{max} * R_{sdson(LOW)} / Iocset
= 1.5 * 14.642 * 5mohm / 10uA
= 11.169K

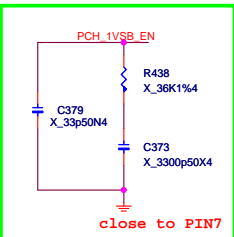
Rocs:11.3K,OCP:

D03-3669S00-F01 : 22.6A

R_{sdson(LOW)} 4.5V

D03-4C05N03-005 : 5 mohm
D03-632BA0C-N03 : 4.6 mohm
D03-3056M00-U47 : 6.2mohm
D03-3669S00-F01 : 5.2m ohm

2014.08.22 close to U34



2015.01.22
for up1540:stuff R438->36K,
C379->NC,C373->3.3nF
for RT8125:R438.C379.C373->NC

2015.01.22
for up1540:R403->2.2R,C362->1uF
for RT8125:R403->10R,C362->1uF

2014.12.25
for up1540:C364&R407 ->NC

2014.12.25
for up1540:C365 is OCP set min:5Kohm
stuff 7.87K OCP SET:15.74A
RT8125C stuff C1000P C11-1022032-W08

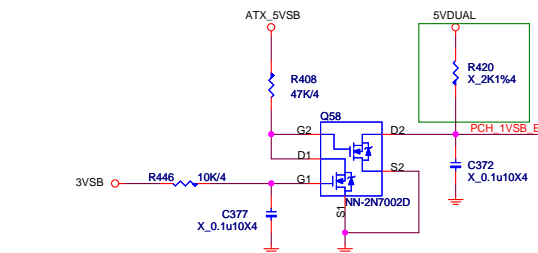
2014.12.25
for up1540:R623 ->NC

38 PCH_CORE_OV << PCH_CORE_OV
to sink/source over voltage IC.
pin10 sink/source current capability can't over 1mA
So max voltage can't over 1.8V.
from NCT3933

from NCT3933

38 PCH_CORE_OV << PCH_CORE_OV

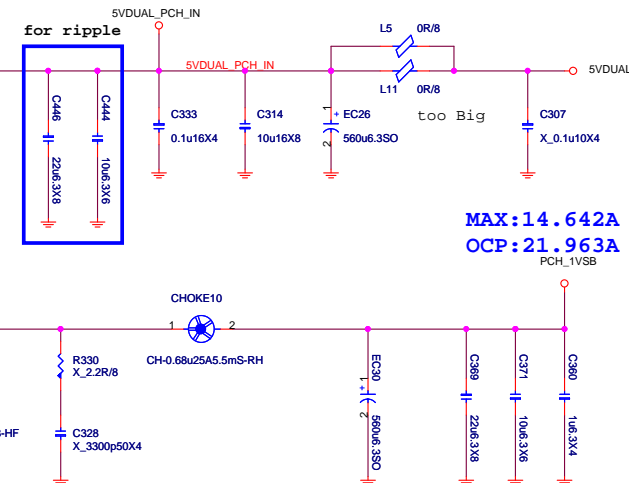
2014.12.25
for up1540:stuff R622->0R



2014.12.25
for up1540:R420 ->NC
RT8125C:R420 ->NC

V_{out} = V_{ref} * (1 + R821/R822)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V

I_{rms} = I_{out} * SQRT((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))
= 14.892 * 0.4
= 5.95686A



MAX:14.642A
OCP:21.963A
PCH_1VSB

I_{min} = ((V_{in} - V_{out})/(F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})
= 0.59689uH (K = 30%)



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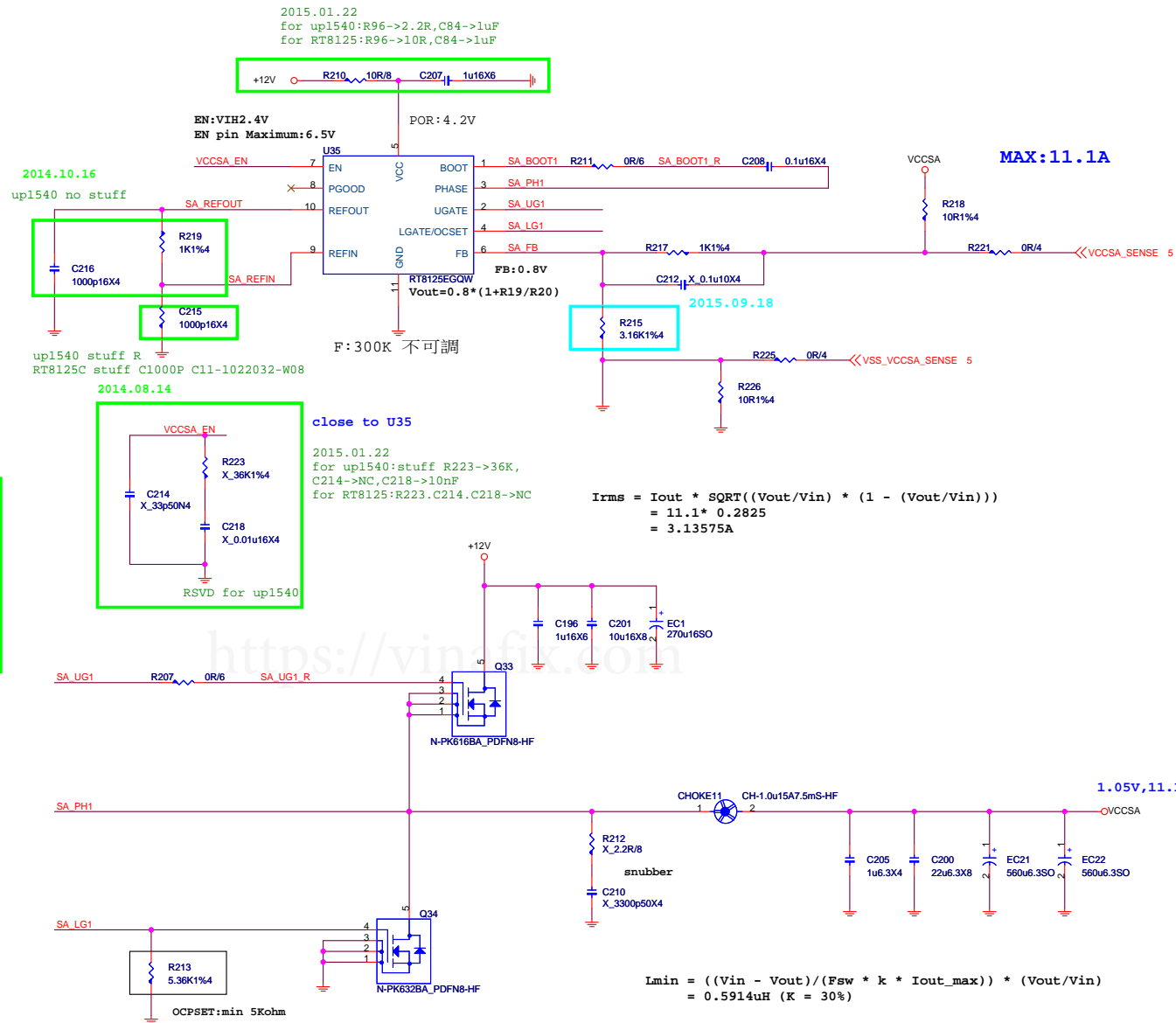
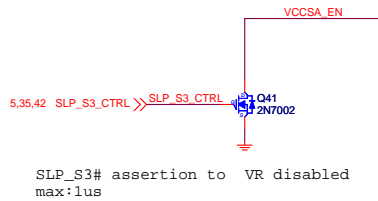
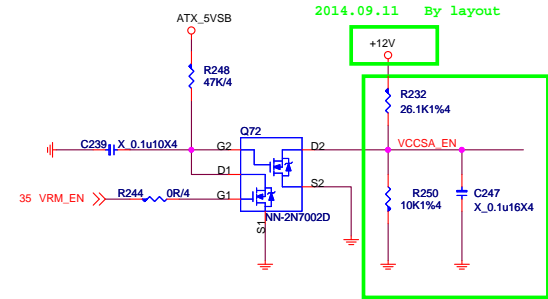
Size	Document Description	Rev
Custom	PCH power - POWER RT8125E	12
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SA Power:1.05V,11.1A

$OCP = 11.1A * 1.4 = 15.54A$
 $R_{cs}(R15) = OCP * R_{dson}(Low\ side) / 10uA$
 $= 15.54 * (3.4)mohm / 10uA$
 $= 5.2836Kohm$

Rcs:5.2836K,OCP:
D03-4C05N03-005 : 15.76A
D03-632BA0C-N03 : 16.24A
use UBIQ MOS need Check

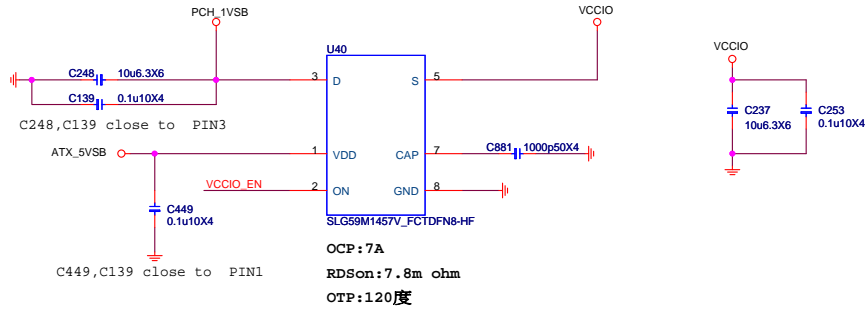
Rdson(Low)10V
D03-4C05N03-005 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm



2015.10.29 change to SLG59M1457 load switch, Pwr source by PCH_1VSB

VCCIO
0.95V; 5.5A
Source 1.00V

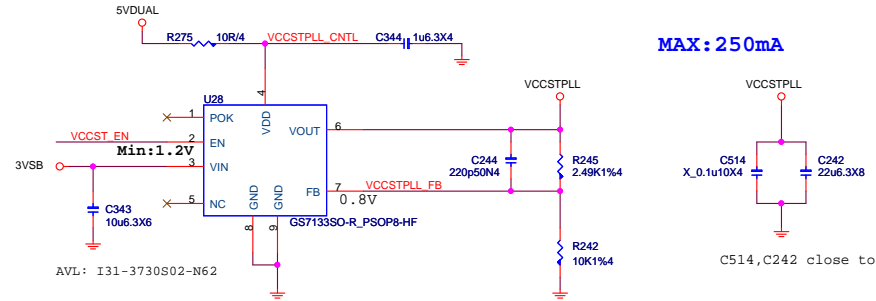
MAX: 5.5A



VCCIO ramped and stable before
beginning of VCCOPC/VCCEPIO ramp

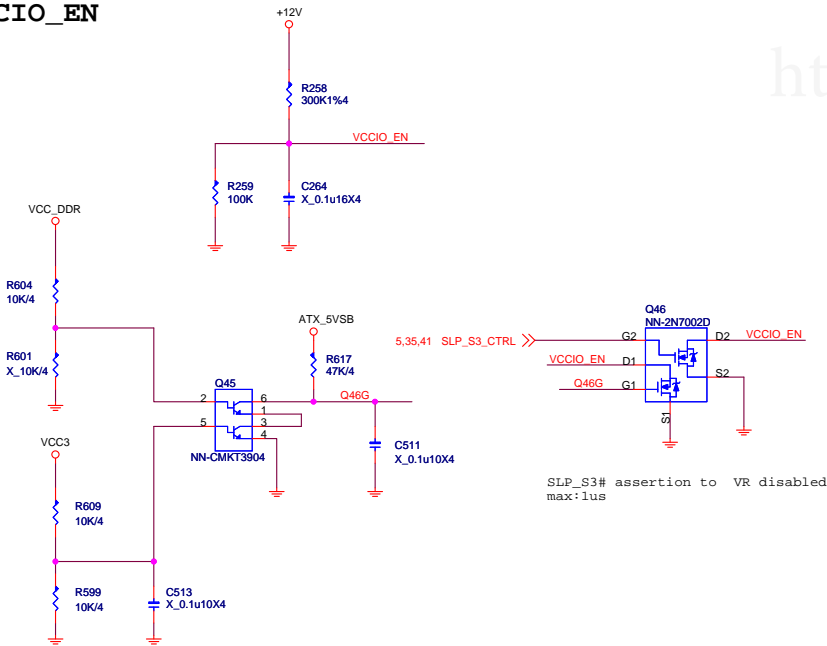
2015.10.29 change to GS7133
VCCSTPLL

MAX: 250mA



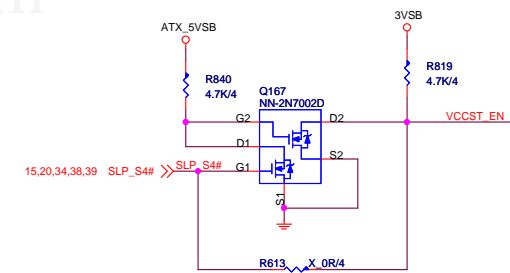
VCCST/PLL stable 1ms before PROCPWRGD

VCCIO_EN



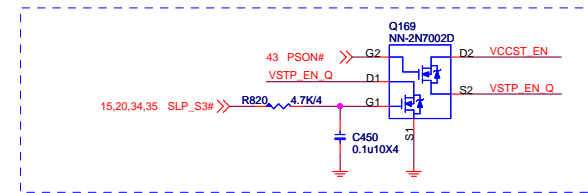
SLP_S3# assertion to VR disabled
max:1us

VCCSTPLL_EN



FIX G3 -> S5 mode VCCSTPLL leakage

2015.12.02

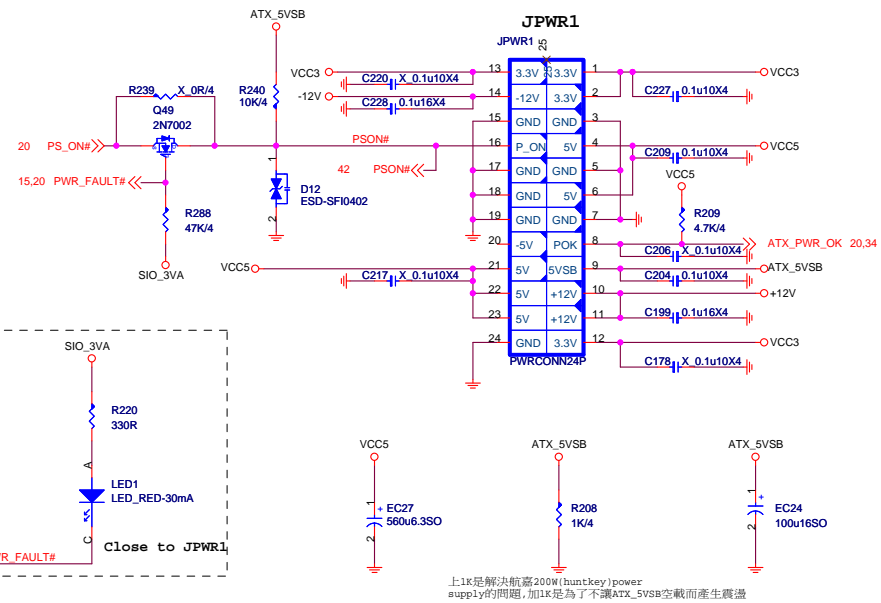


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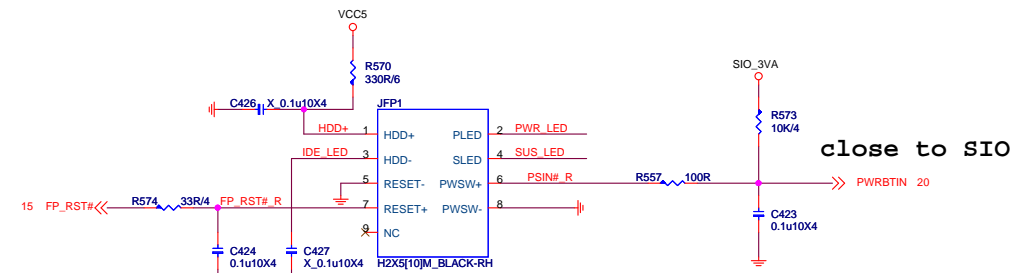
MS-7995

Size Custom	Document Description VCCIO/VCCSTPLL POWER	Rev 12
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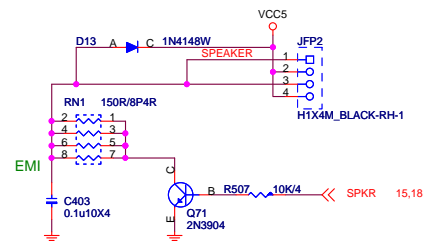
ATX POWER CONNECTOR



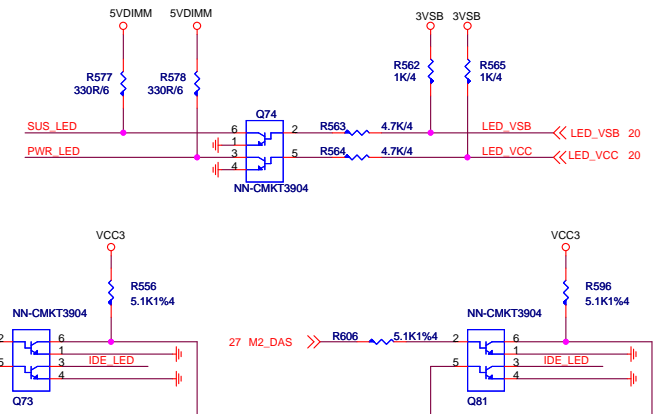
FRONT PANNEL



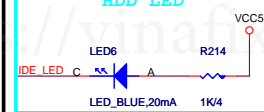
Speaker Pin Header



LED (for NV5563)



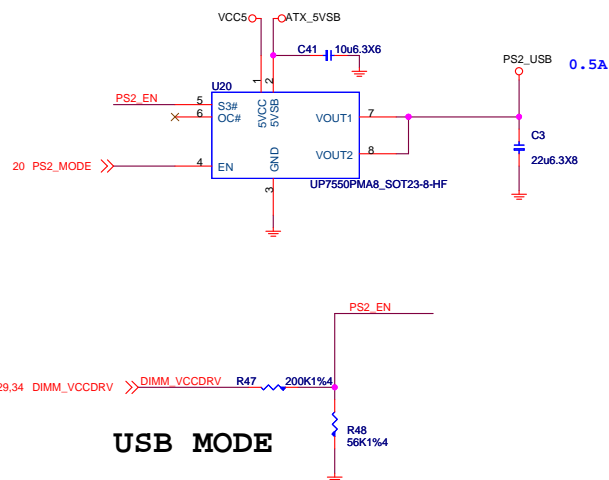
HDD LED



2015.09.21

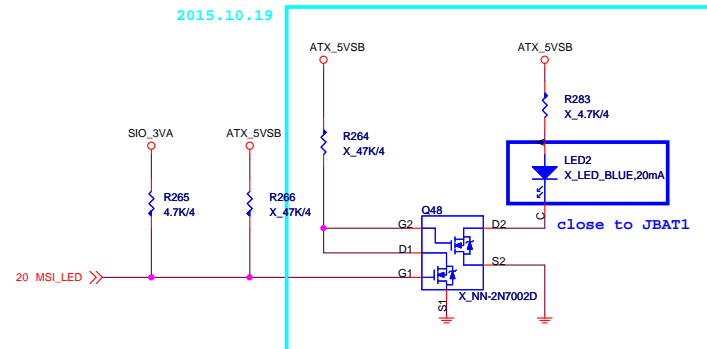
<https://vinafix.com>

PS2 POWER



USB MODE

MSI LED



TPM

Vinafix.com

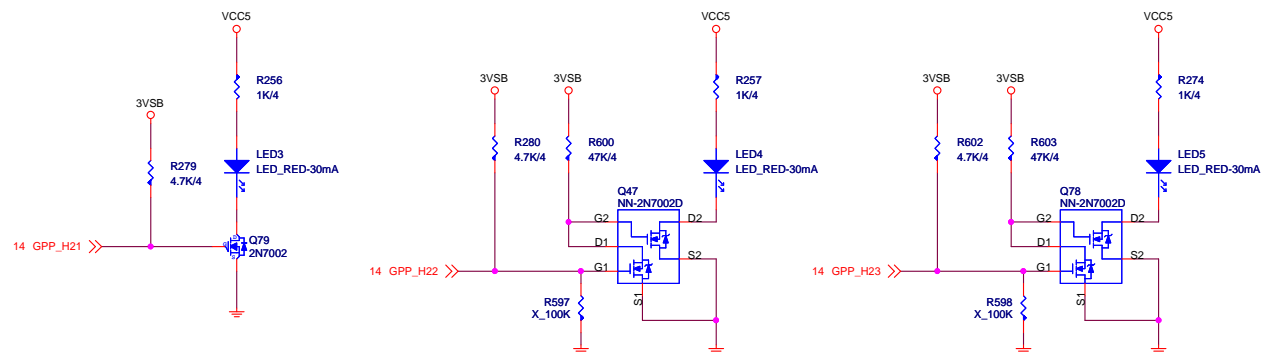


MICRO-STAR INT'L CO.,LTD

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DEBUG LED



GPIO LED	GPP_H21	GPP_H22	GPP_H23
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

關機斷電狀態下，3個LED先維持default全暗，開機通電後：

1. 首先進行CPU check CPU LED 亮，check PASS後則CPU LED減掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED減掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED減掉。
4. 因此最後正常順利開機後，三個LED燈都是減掉的。（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）




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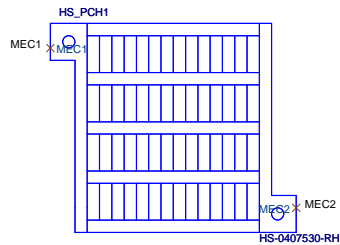
Size Custom	Document Description DEBUG LED	Rev 12
Date: Monday, December 07, 2015		Sheet 44 of 50

EMI CAP

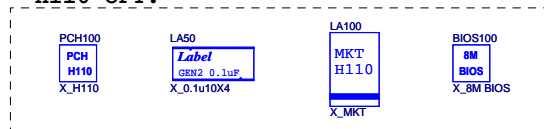
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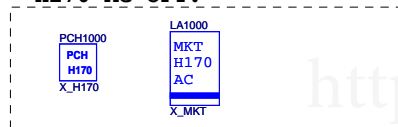
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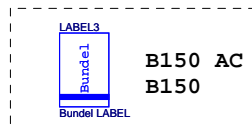
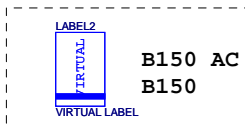
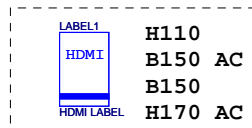
H110 OPT.



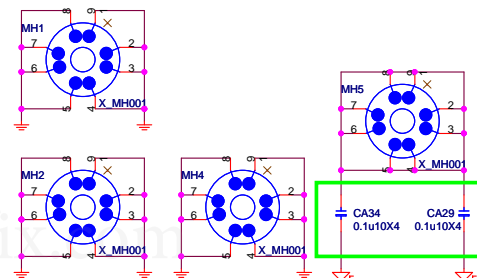
H170 AC OPT.



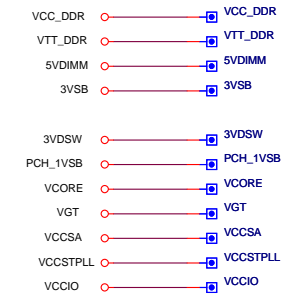
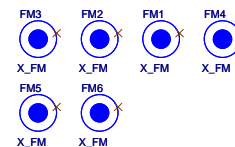
B150 OPT.



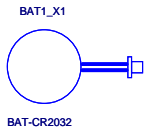
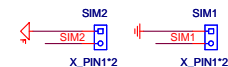
Mounting Holes



Optical Fiducial Marks-120



Simulation



2015/12/8 2015/12/15 PD0-0799512-E48, 競華, 23, 寶安恩斯邁廠 (MSIS) 6, black
2015/12/8 2015/12/15 PD0-0799512-G37, 精成-深圳, 23, 寶安恩斯邁廠 (MSIS) 6, black

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